

Compal Confidential

DIUYA/YB/SA/SB/SD (KBL-R)

DIS M/B Schematics Document

Intel KabyLake U/KabyLake R Processor with DDR4

N16S-GTR(940) (23x23mm)

N16V-GMR1(920) (23x23mm)

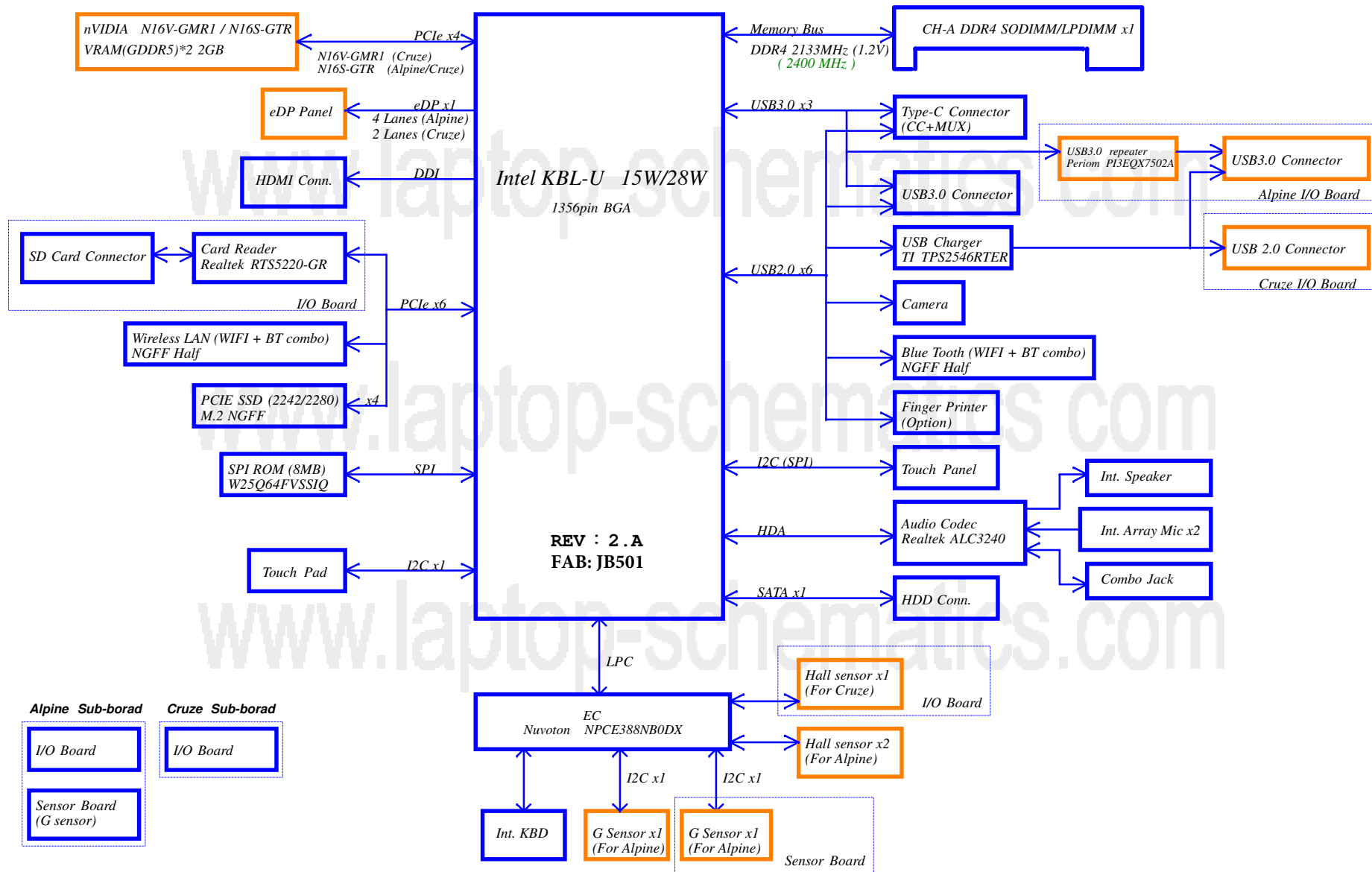
2017-06-05

LA-E541P

REV : 2.A

FAB: JB501

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Voltage Rails

power plane	B+	+5VALW	+1.2V	+5VS +3VS +1.35VS +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG
State		+3VALW		+1.8VS +0.6VS +1.0VALW
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM Structure Table

Item	BOM Structure
For DIS	DIS@
For UMA	UMA@
For Touch Panel with SPI	TS_SPI@
For Touch Panel with I2C	TS_I2C@
For Keyboard backlight	KBL@
No Keyboard backlight	NOKBL@
For Samsung VRAM	S2G@
For Micron VRAM	M2G@
For Hynix VRAM	H2G@
For UHD Panel	UHD@
For Finger Printer	FP@
For SSD	SSD@
For EMI	EMI@
For ESD	ESD@
For RF	RF@
No EMI	@EMI@
No ESD	@ESD@
No RF	@RF@
Connector	ME@
For VARM X76	X76@
For Test Point	TP@
For Debug	@DCI@
For S series only	S_AL@
For S IMR series only	S_IMR@
For YOGA series only	YOGA@
For CPU Type	17_7500U_R1@ 15_7200U_R1@ i3_7100U_R1@ 17_7500U_R3@ 15_7200U_R3@ i3_7100U_R3@ pt_4415U_R1@ pt_4415U_R3@ i3_6006U_R3@

USB 2.0 Port Table

Port	External USB Port
1	USB3 Type-C Port
2	USB2/3 Port (MB)
3	USB2/3 Port (IO/B)
4	USB3 Type-C Port
5	Camera
6	Finger Printer (Option)
7	NGFF WLAN+BT

USB 3.0 Port Table

Port	External USB Port
1	USB3 Type-C (MUX)
2	USB2/3 Port (MB)
3	USB2/3 Port (IO/B)
4	
5	
6	

SATA Port Table

Port	External SATA Port
0	HDD
1	

PCIe Port Table

Lane	Port	External PCIe Port
1		
2		
3	1	GPU
4		
5		
6		
7		Card Reader NGFF WLAN+BT
8		
9		
10		
11	3	SSD
12		

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x 16h

EC SM Bus2 address

Device	Address
NC7718W	1001 100x 98h

EC SM Bus4 address

Device	Address
BMA250E	0001 100x 18h

PCH SM Bus address

Device	Address
DOR_JDIMM1 Touch Pad	1010 000x A0h

GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111x 9Eh

SMBUS Control Table

	SOURCE	VGA	BATT	CHARGER	NECP388	SODIMM	Thermal Sensor	DGPU			TP	PCH	G-SENSOR
SMB_EC_CK1	NECP388	X	V	V	X	X	X	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW	+19V_VIN									
SMB_EC_CK2	NECP388	X	X	X	X	X	X	X	X	X	X	X	X
SMB_EC_DA2	+3VGS		+3VGS		+3VS		+3VS				+3VS		
SMB_EC_CK4	NECP388	X	X	X	X	X	X	X	X	X	X	X	X
SMB_EC_DA4	+3VALW												+3VS
PCH_SMBCLK	PCH	X	X	X	X	X	X	X	X	X	X	X	X
PCH_SMBDATA	+3VALW										+3VS		
SML0CLK	PCH	X	X	X	X	X	X	X	X	X	X	X	X
SML0DATA	+3VALW										+3VS		
SML1CLK	PCH	X	X	X	X	X	X	X	X	X	X	X	X
SML1DATA	+3VALW										+3VS		

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

X4E

Yoga Series

ZZZ4 X4E_YA@	ZZZ3 X4E_YA_FP@	ZZZ5 X4E_YB@	ZZZ6 X4E_YB_FP@
X4E Y Series X4EASR38L1	X4E Y Series FP SKU X4EASR38L2	X4E Y Series UHD SKU X4EASR38L2	X4E Y Series UHD&FP SKU X4EASR38L1

S Series

ZZZ7 X4E_S@	ZZZ7 X4E_S_FP@
X4E S Series X4EASR38L1	X4E S Series FP SKU X4EASR38L2

HDMI Logo

ZZZ 45@
HDMI Logo RC0000003HM

Yoga Series (U42)

ZZZ X4E_U42_YA@	ZZZ X4E_U42_YA_FP@	ZZZ1 X4E_U42_YB@	ZZZ2 X4E_U42_YB_FP@
X4E Y Series X4EASR38L1	X4E Y Series FP SKU X4EASR38L1	X4E Y Series UHD SKU X4EASR38L2	X4E Y Series UHD&FP SKU X4EASR38L1

S Series (U42)

ZZZ X4E_U42_S@	ZZZ X4E_U42_S_FP@
X4E S Series X4EASR38L1	X4E S Series FP SKU X4EASR38L2

PCB part

ZZZ YOGA@
PCB Y Series DA00019512A
ZZZ S_AL@
PCB S Series DA00019512A
ZZZ S_IMR@
PCB S Series DA00019512A

GDDR5 VRAM * 2

X7671138L03

U6 S2G@	U7 S2G@
K4G80325FB-HC03 SA000094R20	K4G80325FB-HC03 SA000094R20
RV65 SDQ3449180 1.99K_0402_1% S2G@	RV65 SDQ3449180 1.99K_0402_1% S2G@

X7671138L02

U6 M2G@	U7 M2G@
MT51J256M32HF SA000096R20	MT51J256M32HF SA000096R20
RV65 SDQ3449180 1.99K_0402_1% M2G@	RV65 SDQ3449180 1.99K_0402_1% M2G@

X7671138L01

U6 H2G@	U7 H2G@
H5GCB24MUR-T2C SA000092G10	H5GCB24MUR-T2C SA000092G10
RV65 SDQ3449180 30.1K_0402_1% H2G@	RV65 SDQ3449180 30.1K_0402_1% H2G@

GPU part

U1 N16S_R1@	U1 N16V_R1@
N16S-GTR-S-A2 BGA 595P SA000097P00	N16V-GMR1-S-A2 BGA 595P SA000097T00
U1 N16S_R3@	U1 N16V_R3@
N16S-GTR-S-A2 BGA 595P SA000097P00	N16V-GMR1-S-A2 BGA 595P SA000097T00

CPU part

KBL U22 (= U22@)

U1 i3_7100U_R1@	U1 i5_7200U_R1@	U1 i7_7500U_R1@	U1 i7_4415U_R1@
QLYKH0 2.4G SA0000A38A0	QLYYH0 2.5G SA0000A37A0	QLYYH0 2.7G SA0000A37A0	QLYYH0 2.9G SA0000ADV00
U1 i3_7100U_R3@	U1 i5_7200U_R3@	U1 i7_7500U_R3@	U1 i7_4415U_R3@
SR343 H0 2.4G SA0000A38B0	SR342 H0 2.5G SA0000A37B0	SR341 H0 2.7G SA0000A34A0	SR348 H0 2.9G SA0000ADV20

SKL U22 (= U22@)

U1 i3_6006U_R3@
SR2JG R1 i3-6006U 2.0G C381 SA0000ACN10

KBL U42 (= U42@)

U1 i5_QNFB_R1@	U1 i7_QNFB_R1@
QNEFY0 1.6G FCBGA SA0000AWB00	QNEFY0 1.6G FCBGA SA0000AWC00
U1 i5_QNFB_R3@	U1 i7_QNFB_R3@
QNEFY0 1.6G FCBGA SA0000AWB50	QNEFY0 1.6G FCBGA SA0000AWC50

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Notes List

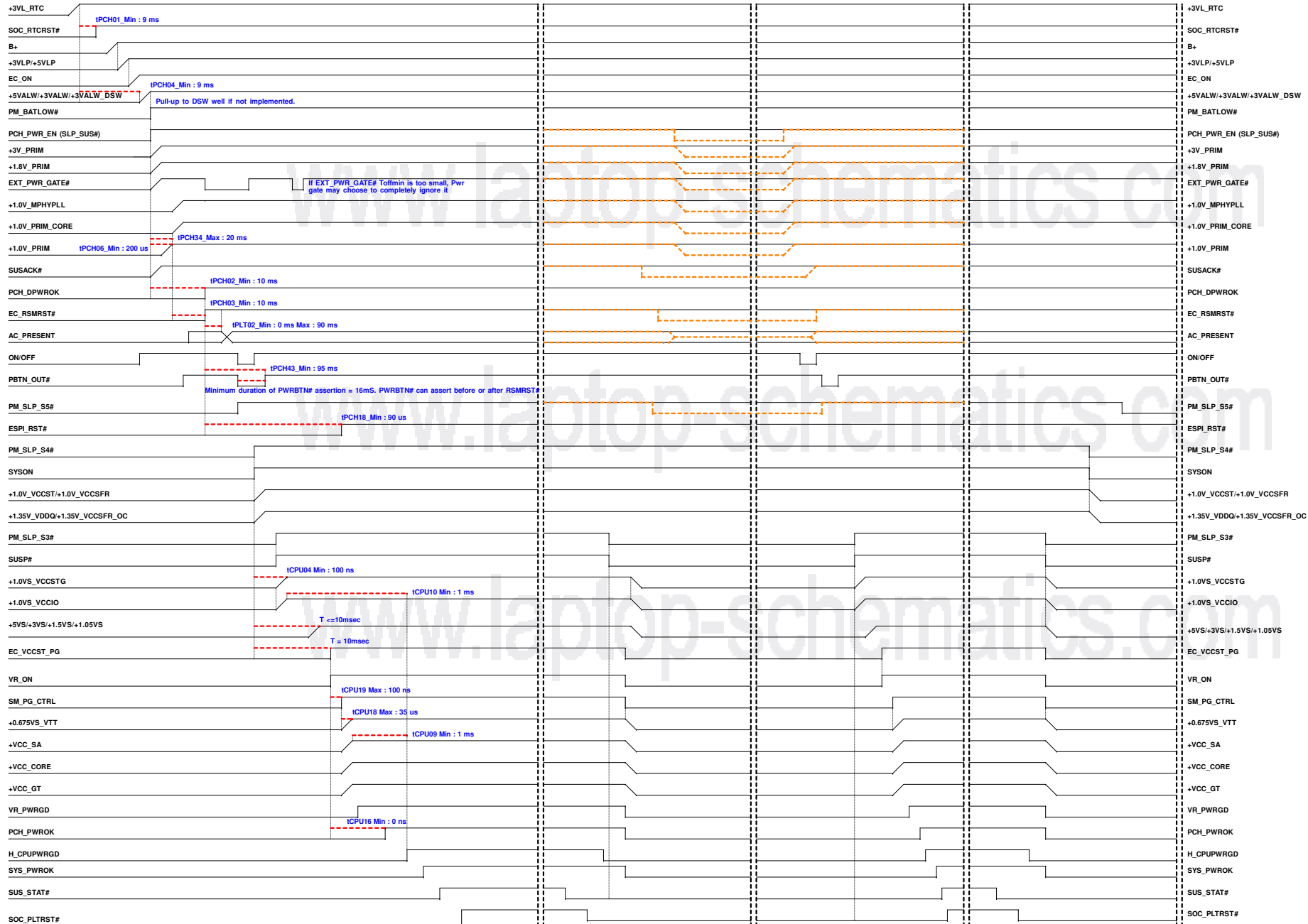
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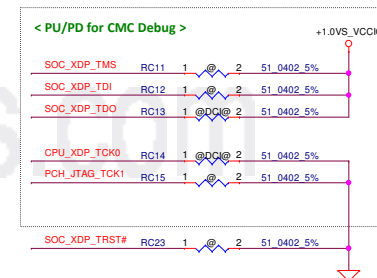
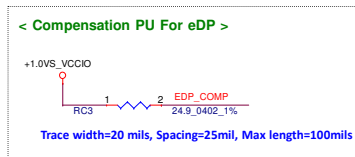
G3→S0

S0→S3/DS3

S0/DS3→S0

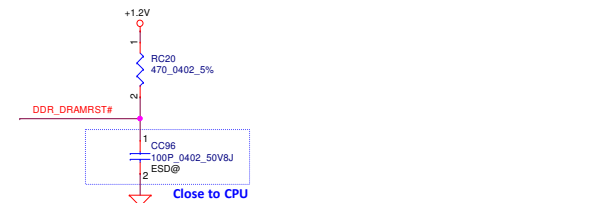
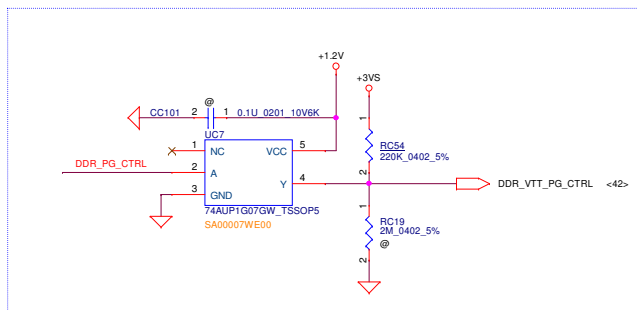
S0→S5





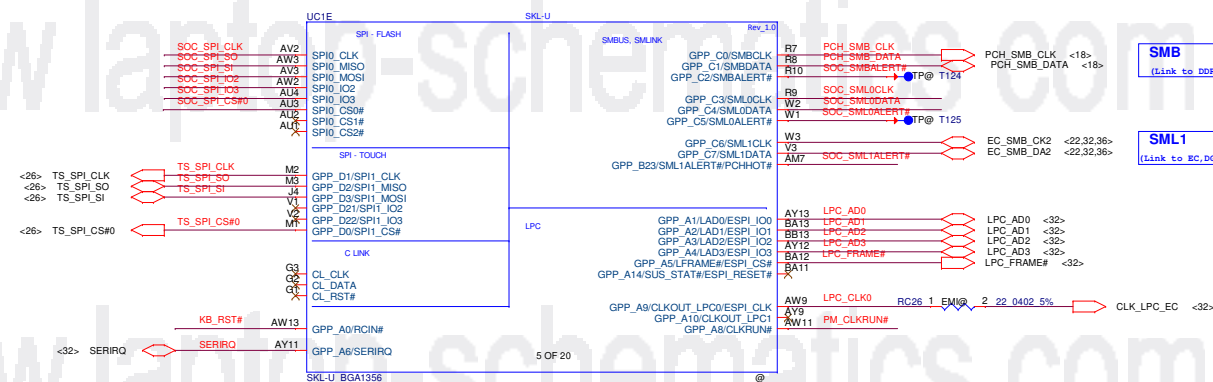
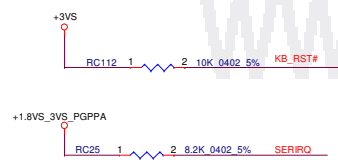
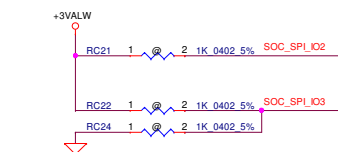
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Interleaved Memory

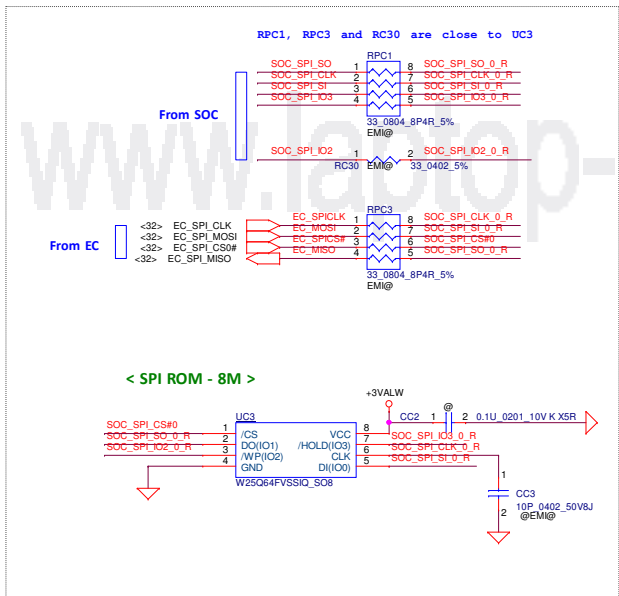
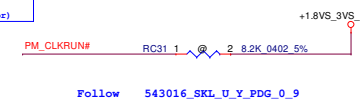
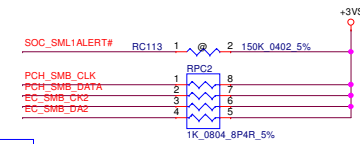
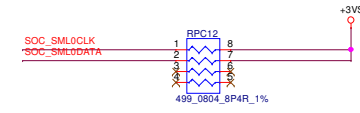


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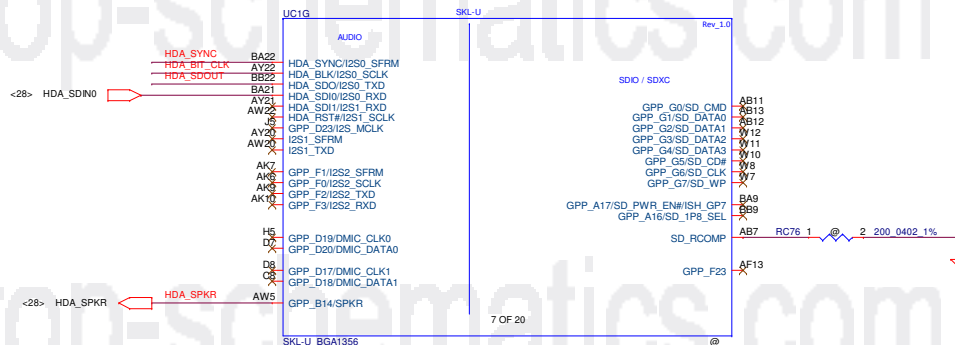
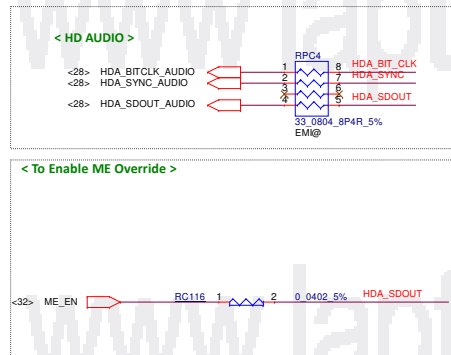
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SKL-U(2/12)DDR3L	
LA-E541P	



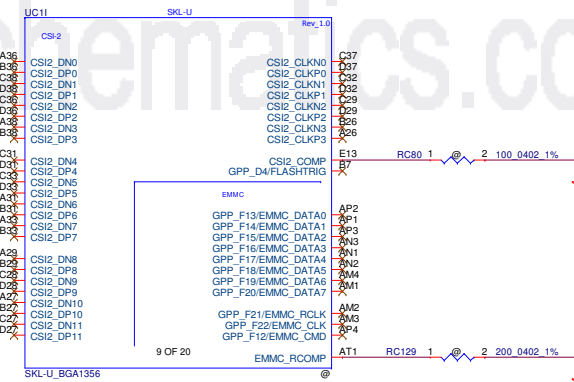
SML0ALERT# (Internal Pull Down):
eSPI or LPC
0 = LPC is selected for EC ==> Default
1 = eSPI is selected for EC



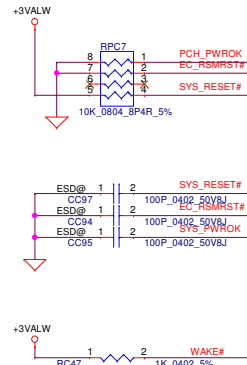
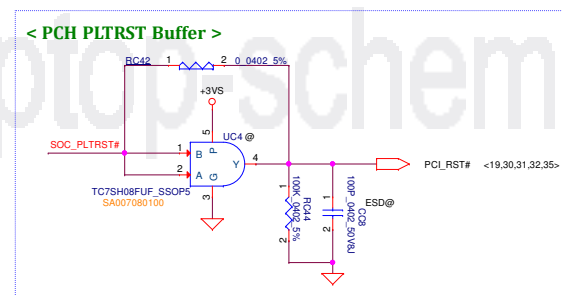
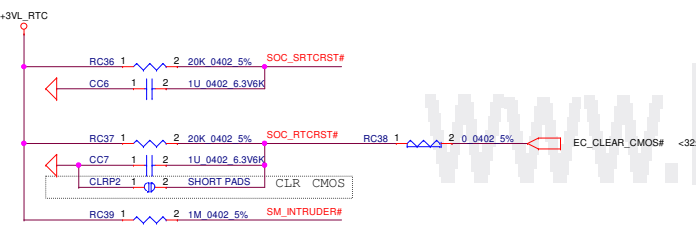
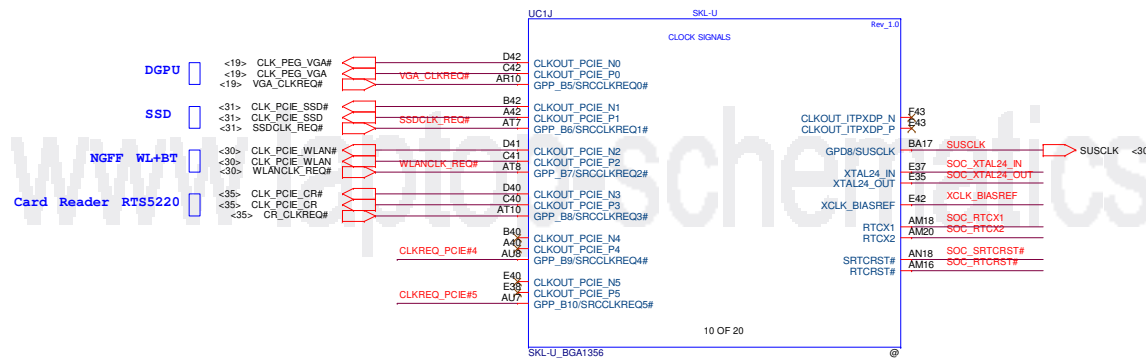
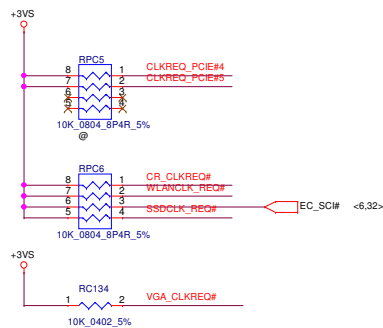
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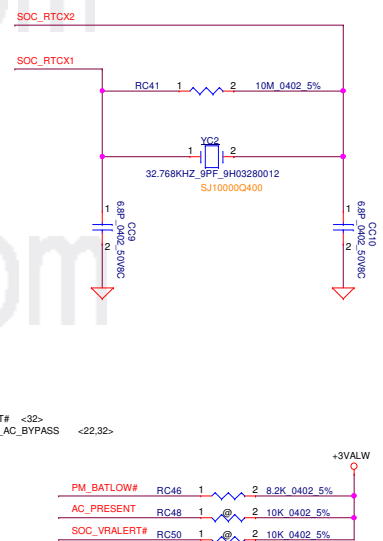
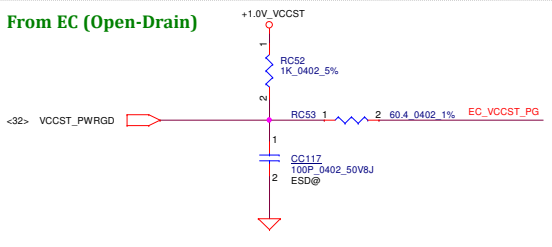
SPKR (Internal Pull Down):
TOP Swap Override
0 = Disable TOP Swap mode. ==> Default
1 = Enable TOP Swap Mode.



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Only For Power Sequence Debug



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GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

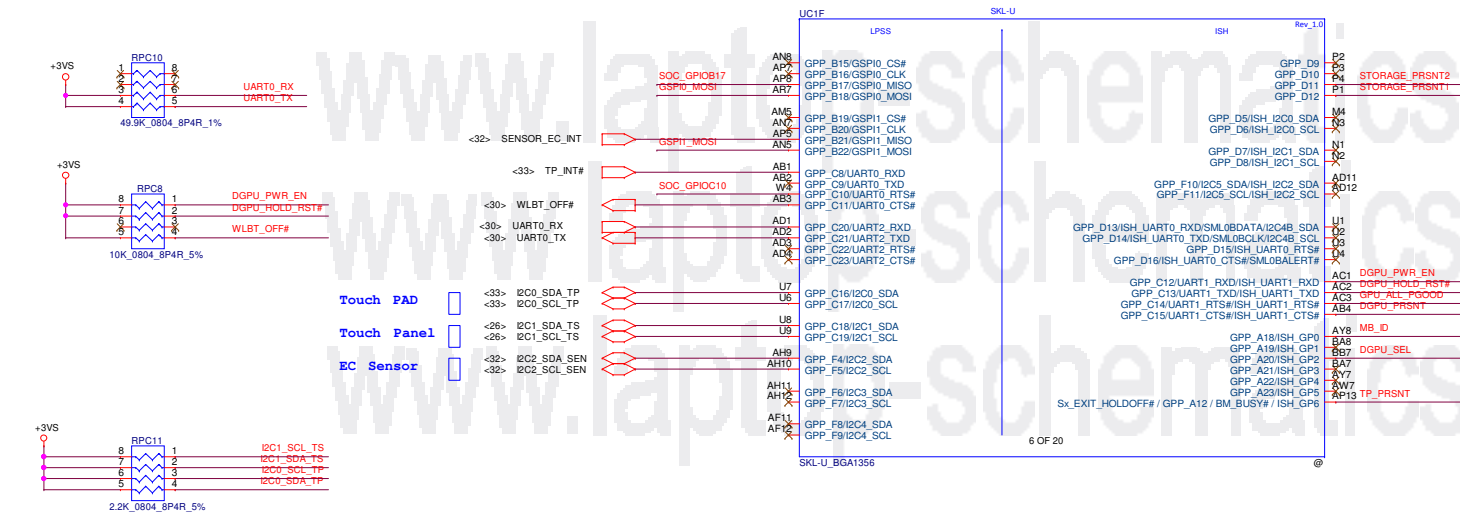
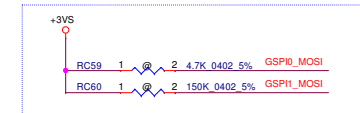
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is used when running ITP/XDP.

GSPI1_MOSI (Internal Pull Down):

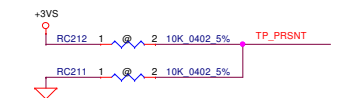
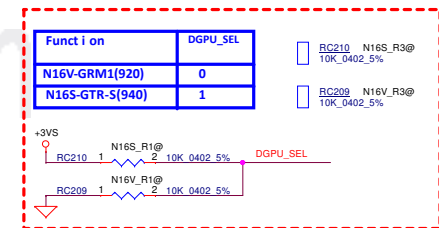
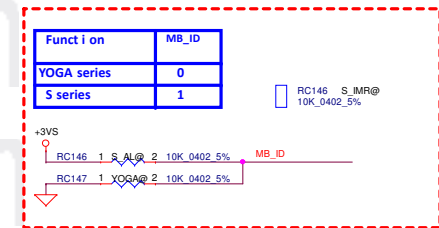
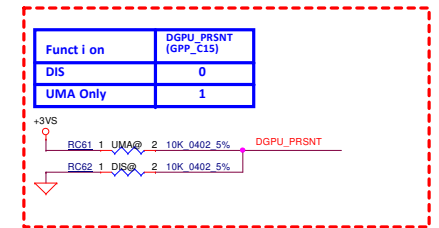
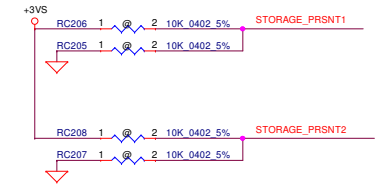
Boot BIOS Strap Bit

0 = SPI Mode ==> Default

1 = LPC Mode



TO DGPU



<19> PCIE_PRX_DTX_N1
<19> PCIE_PRX_DTX_P1
<19> PCIE_PTX_C_DRX_N1
<19> PCIE_PTX_C_DRX_P1

<19> PCIE_PRX_DTX_N2
<19> PCIE_PRX_DTX_P2
<19> PCIE_PTX_C_DRX_N2
<19> PCIE_PTX_C_DRX_P2

<19> PCIE_PRX_DTX_N3
<19> PCIE_PRX_DTX_P3
<19> PCIE_PTX_C_DRX_N3
<19> PCIE_PTX_C_DRX_P3

<19> PCIE_PRX_DTX_N4
<19> PCIE_PRX_DTX_P4
<19> PCIE_PTX_C_DRX_N4
<19> PCIE_PTX_C_DRX_P4

Card Reader

NGFF WLAN+BT

HDD

<31> PCIE_PRX_DTX_N9
<31> PCIE_PRX_DTX_P9
<31> PCIE_PTX_C_DRX_N9
<31> PCIE_PTX_C_DRX_P9

<31> PCIE_PRX_DTX_N10
<31> PCIE_PRX_DTX_P10
<31> PCIE_PTX_C_DRX_N10
<31> PCIE_PTX_C_DRX_P10

SSD

<31> PCIE_PRX_DTX_N11
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<31> PCIE_PTX_C_DRX_N11
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<31> PCIE_PRX_DTX_P12
<31> PCIE_PTX_C_DRX_N12
<31> PCIE_PTX_C_DRX_P12

CC11 DIS@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_N1
CC14 DIS@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_P1

CC15 DIS@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_N2
CC16 DIS@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_P2

CC18 DIS@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_N3
CC13 DIS@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_P3

CC17 DIS@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_N4
CC18 DIS@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_P4

CC19 1 2 0.1U 0201 10V K XSR PCIE_PTX_DRX_N5
CC20 1 2 0.1U 0201 10V K XSR PCIE_PTX_DRX_P5

CC102 1 2 0.1U 0201 10V K XSR PCIE_PTX_DRX_N6
CC103 1 2 0.1U 0201 10V K XSR PCIE_PTX_DRX_P6

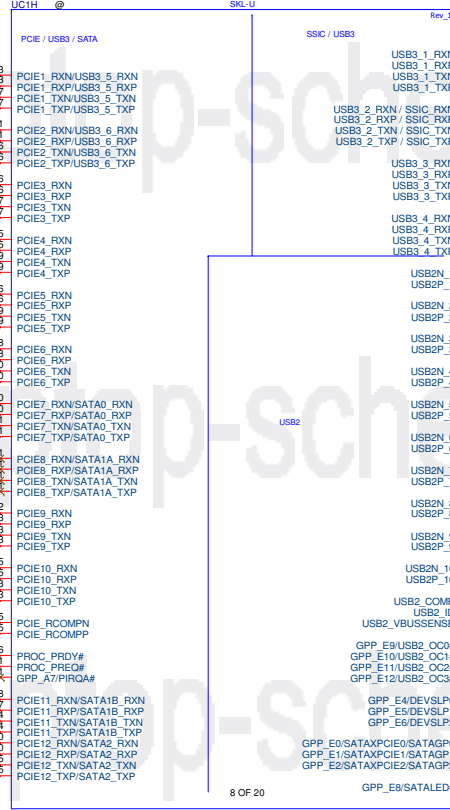
CC110 SSD@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_N9
CC109 SSD@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_P9

CC114 SSD@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_N10
CC113 SSD@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_P10

RC71 1 2 100 0402 1% PCIE_ROMPN
PCIE_ROMMP

CC116 SSD@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_N11
CC115 SSD@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_P11

CC112 SSD@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_N12
CC111 SSD@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_P12



USB3 Type-C (MUX)

USB2/3 Port (MB)

USB2/3 Port (IO/B)

USB3 Type-C Port

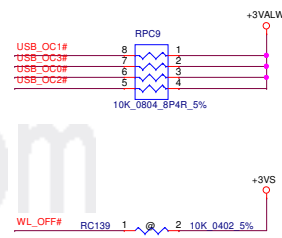
USB2/3 Port (MB)

USB2/3 Port (IO/B)

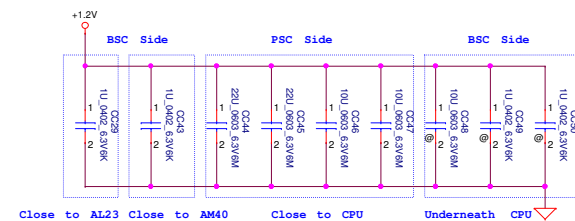
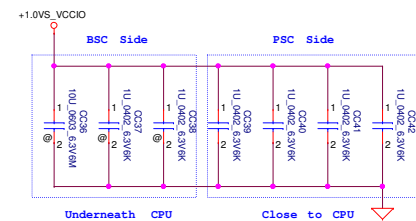
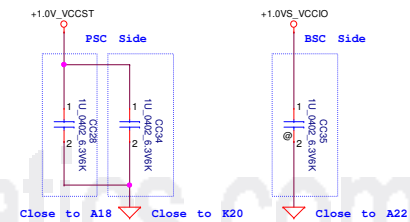
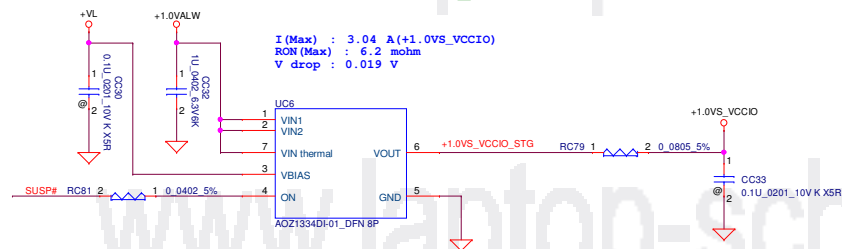
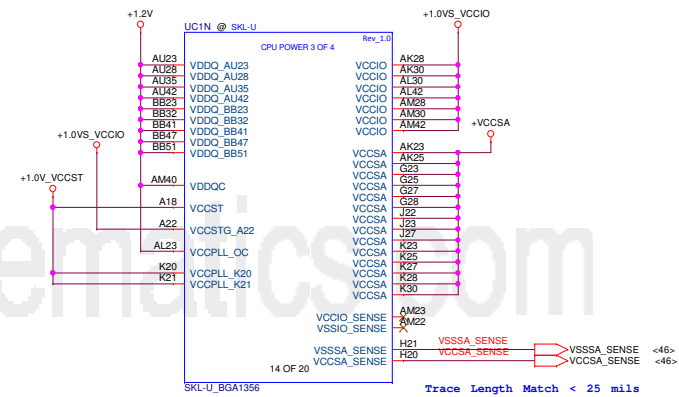
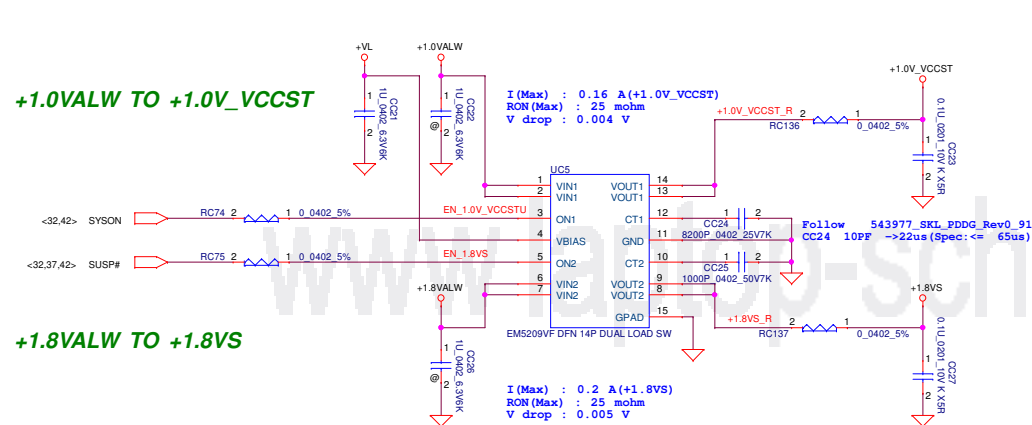
Camera

Finger Printer

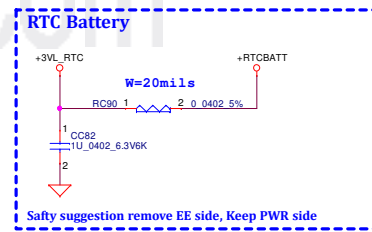
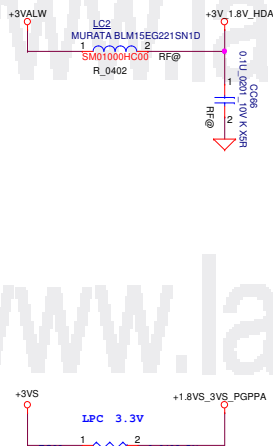
NGFF WLAN+BT



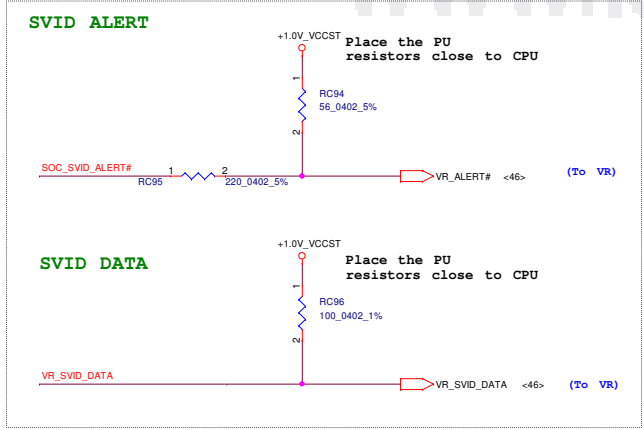
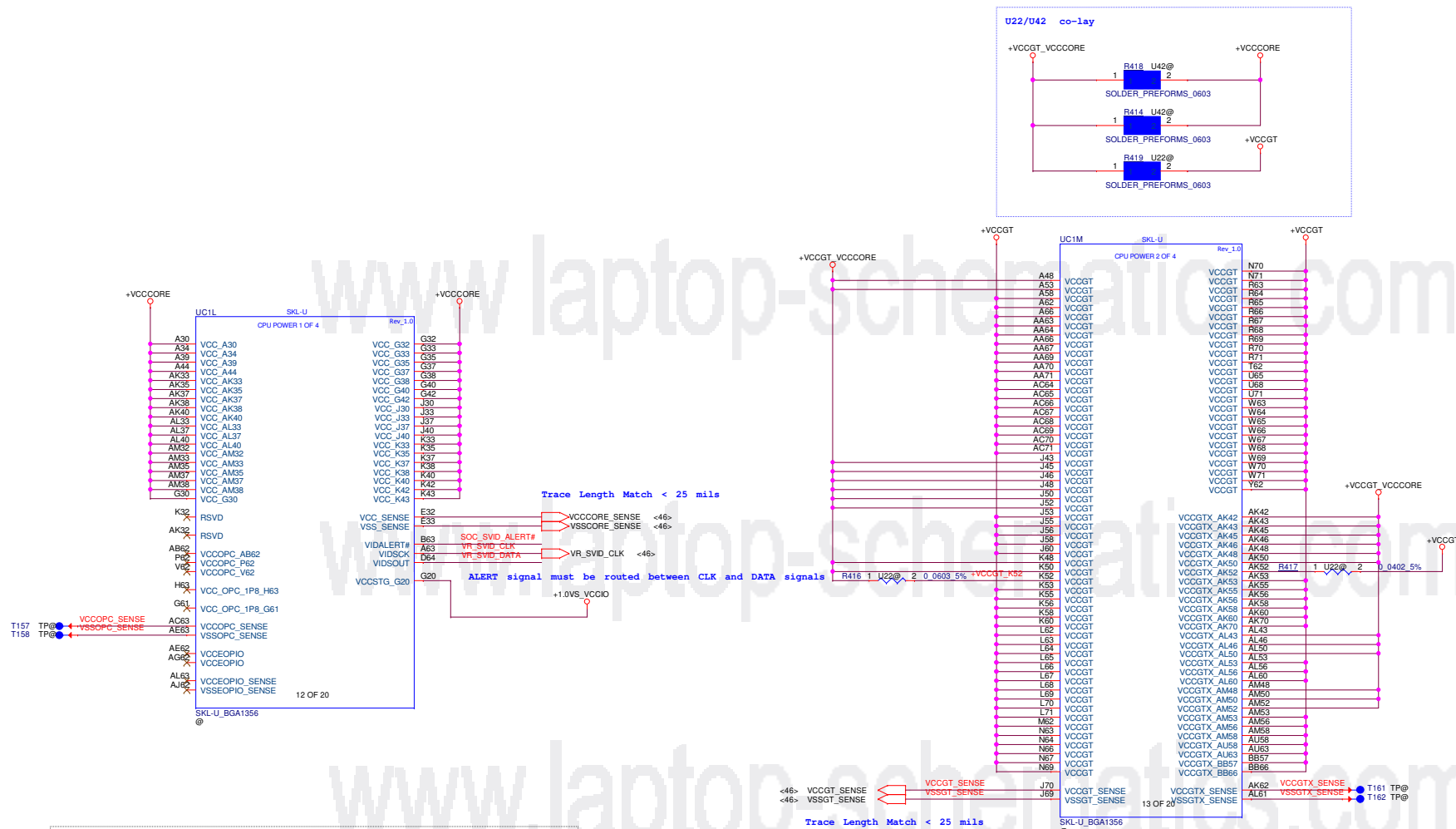
When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.



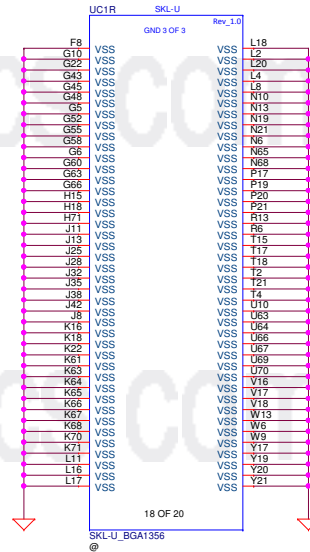
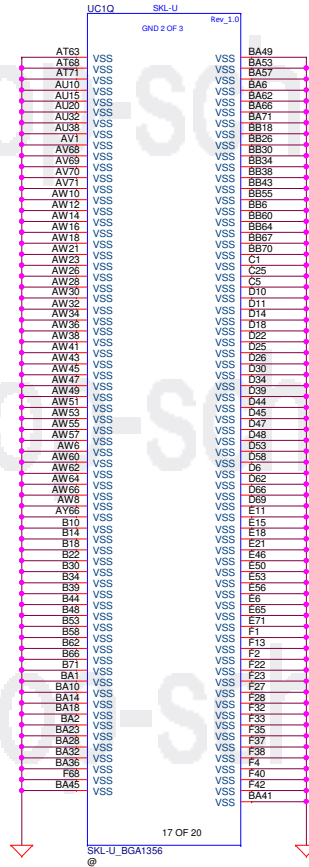
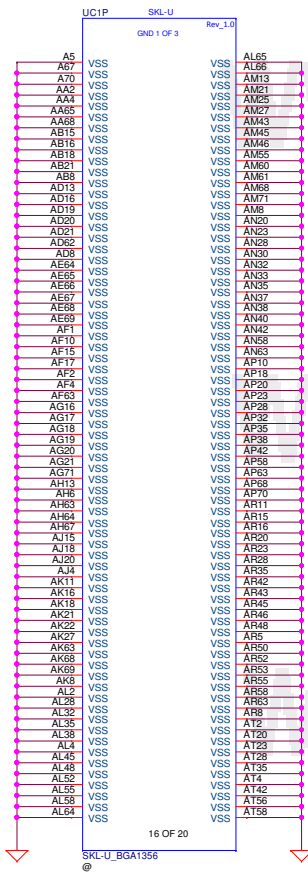
Security Classification		Compal Secret Data		Compal Electronics, Inc. SKL-U(8/12)Power		
Issued Date	2017/06/05	Deciphered Date	2018/06/05	Title		
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				Custom	LA-E541P	2A
				Date:	Wednesday, June 21, 2017	Sheet 13 of 51



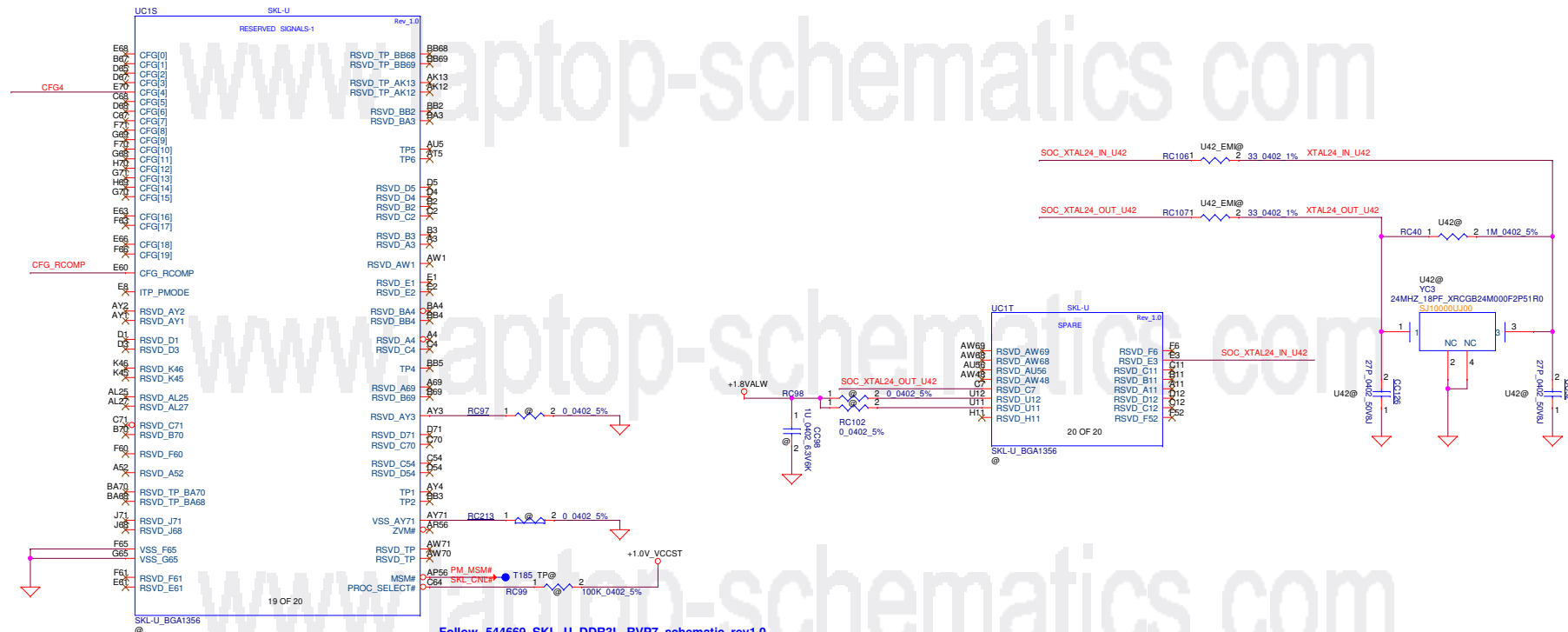
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Issued Date	2017/06/05	Deciphered Date	2018/06/05	Title	SKL-U(9/12)Power	
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				Custom	LA-E541P	
				Date:	Wednesday, June 21, 2017	Sheet 14 of 51



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Issued Date	2017/06/05	Deciphered Date	2018/06/05	Title	
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				Custom	LA-E541P
				Date:	Wednesday, June 21, 2017
				Sheet	15 of 51
				Rev	2A



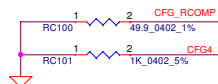
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Issued Date	2017/06/05	Deciphered Date	2018/06/05	Title	
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Size	Document	Number	Rev	2.A	
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Follow 544669_SKL_U_DDR3L_RVP7_schematic_rev1.0

Stuff 100k(RC99) for CannonLake-U

Un-stuff 100k(RC99) for SkyLake-U



Display Port Presence Strap

CFG4

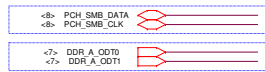
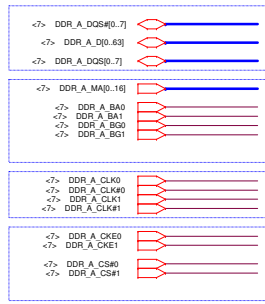
1 : Disabled;
No Physical Display Port attached to Embedded Display Port

0 : Enabled;
An external Display Port device is connected to the Embedded Display Port

Security Classification		Compal Secret Data		Title	
Issued Date	2017/06/05	Deciphered Date	2018/06/05	SKL-U(12/12)CFG,RSVD	
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				Document Number	2A
				LA-E541P	
				Date:	Wednesday, June 21, 2017
				Sheet	17 of 51

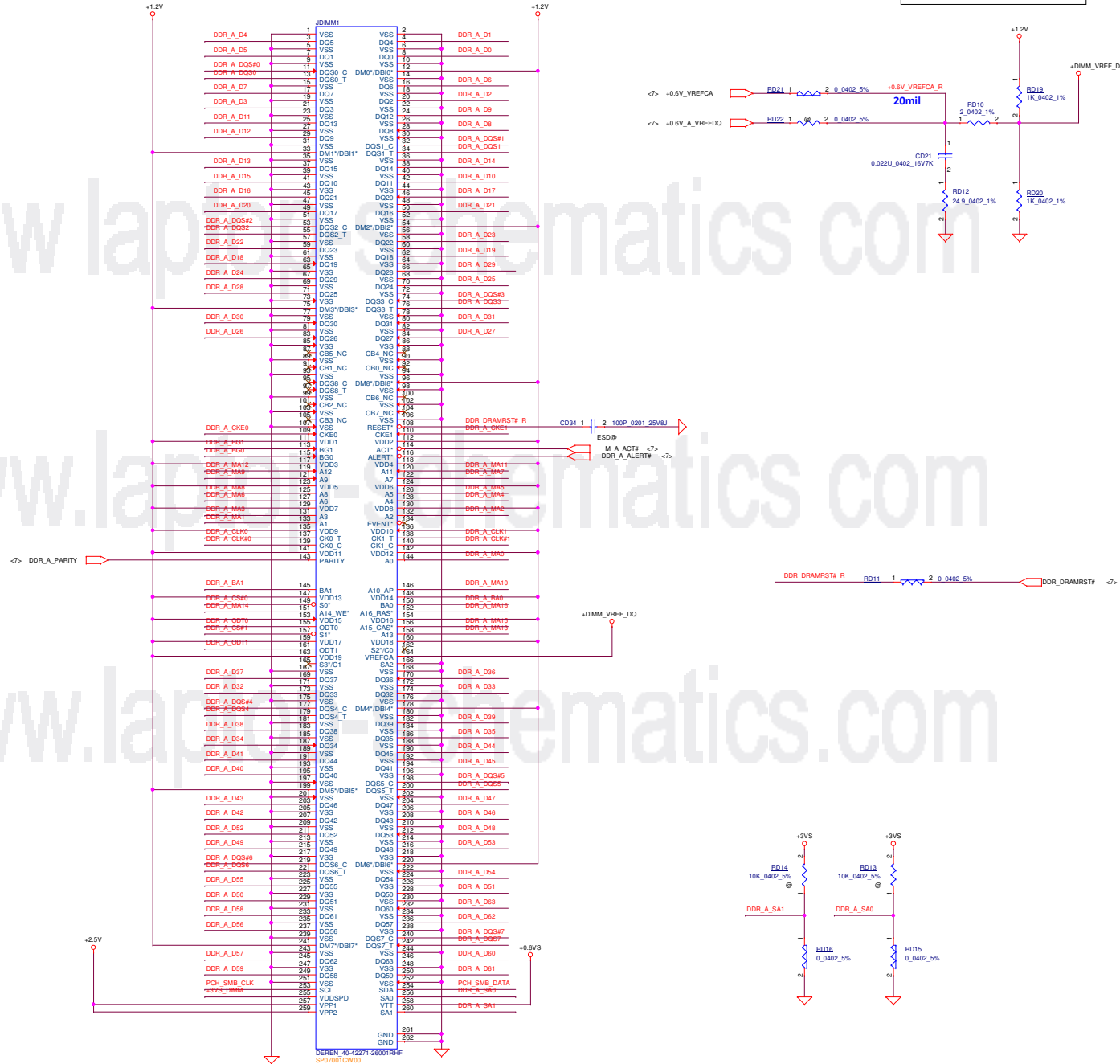
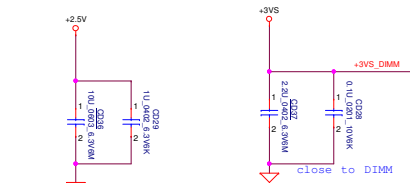
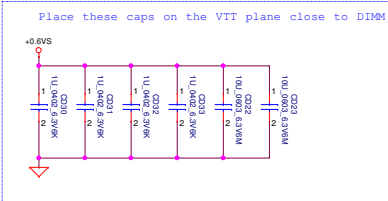
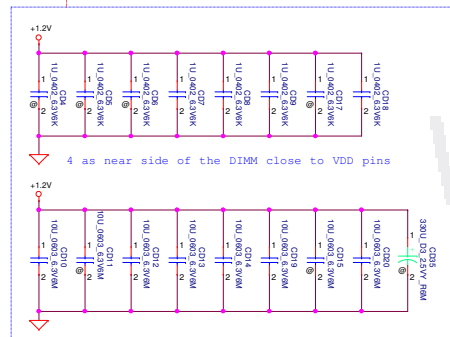
Interleaved Memory

Reverse Type
2-3A to 1 DIMMs/channel

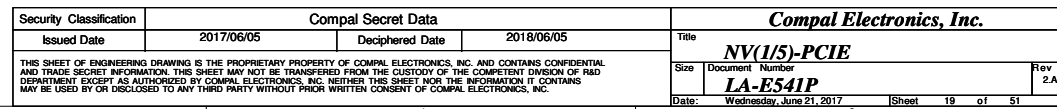
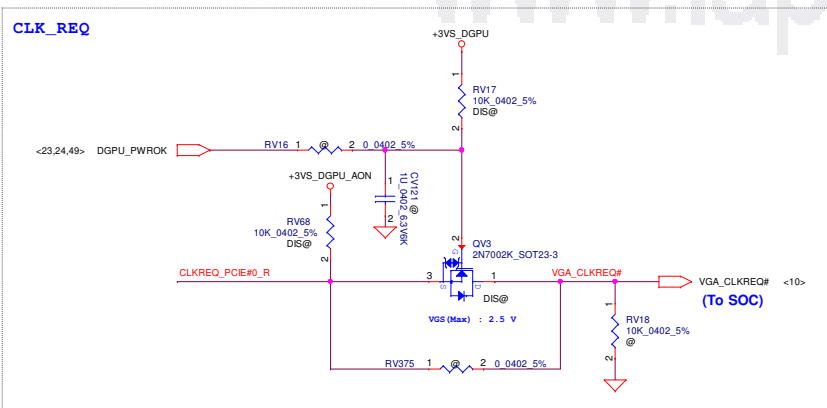
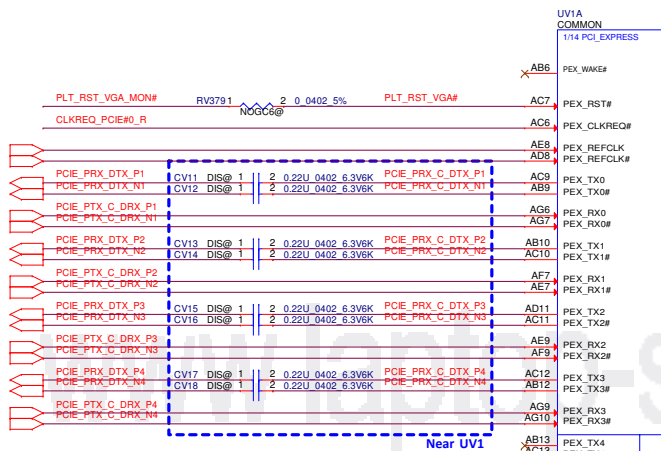


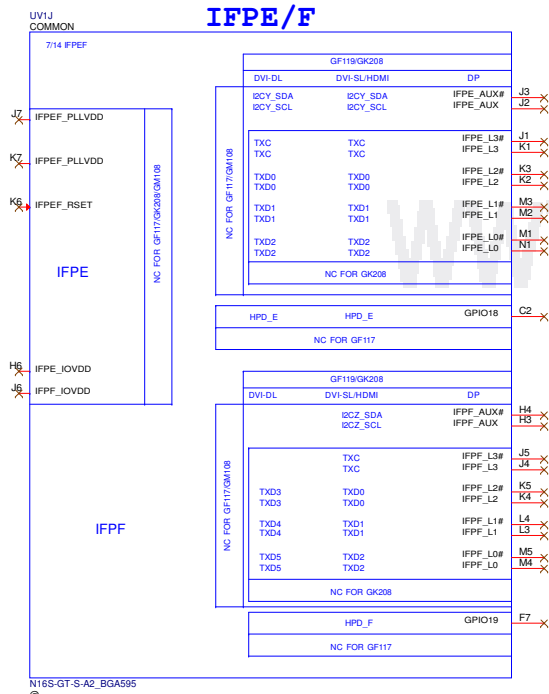
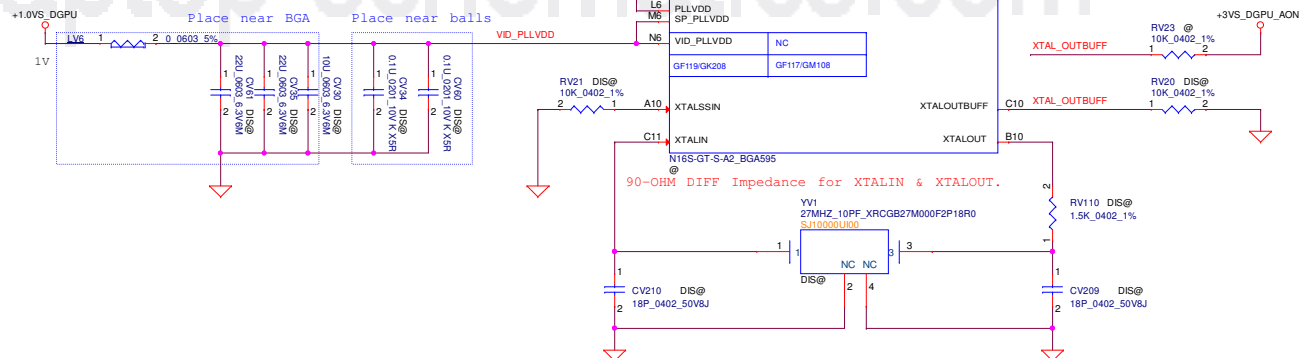
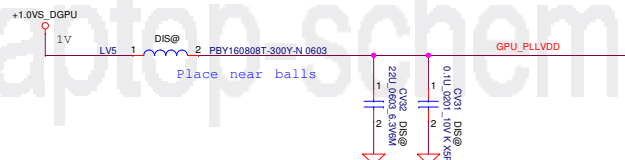
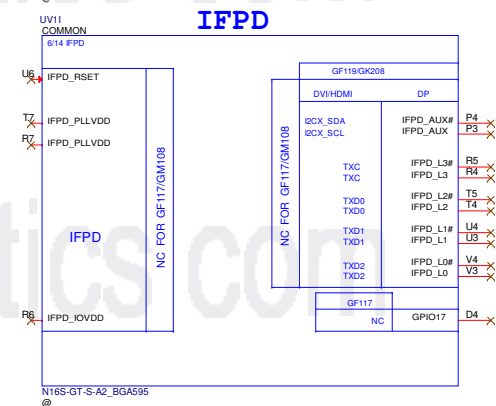
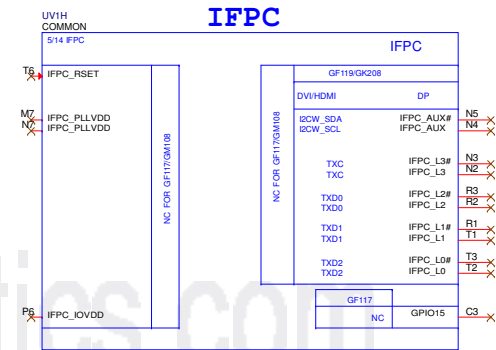
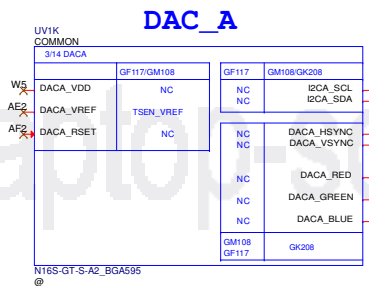
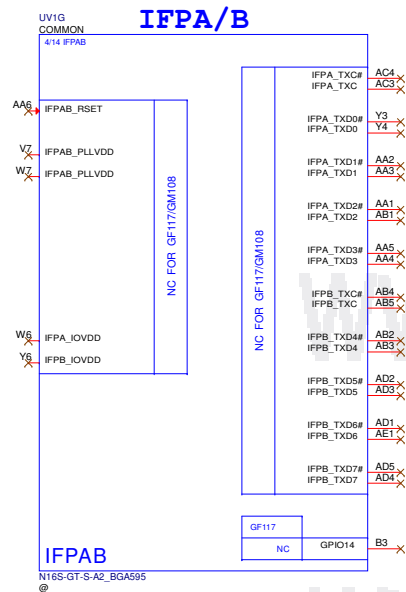
Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

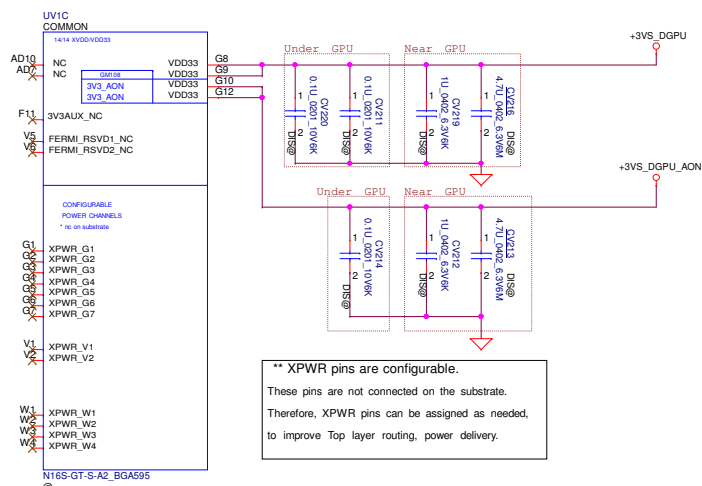
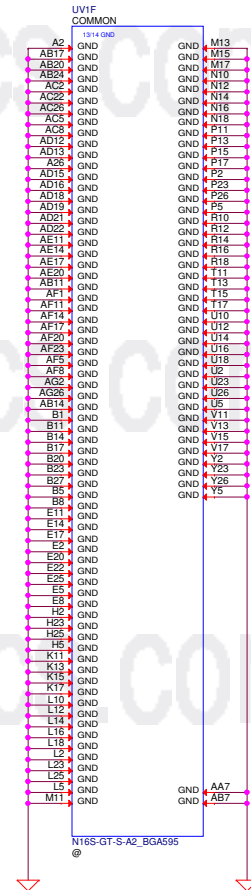
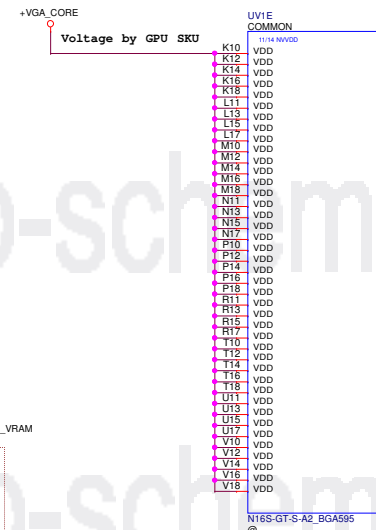
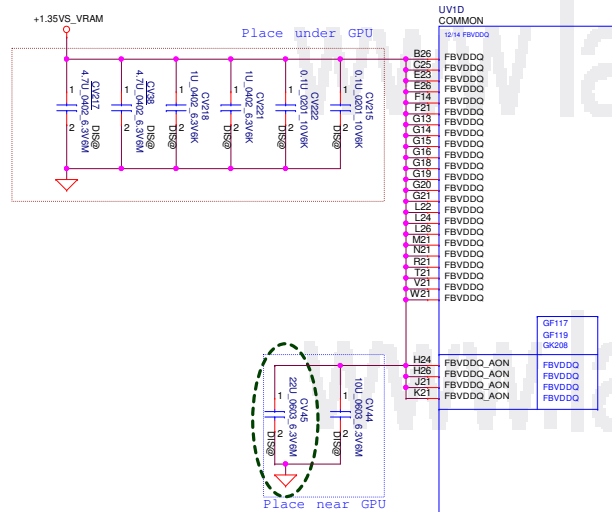


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Rev 2A				Date: Wednesday, June 21, 2017	
Sheet 18 of 51					



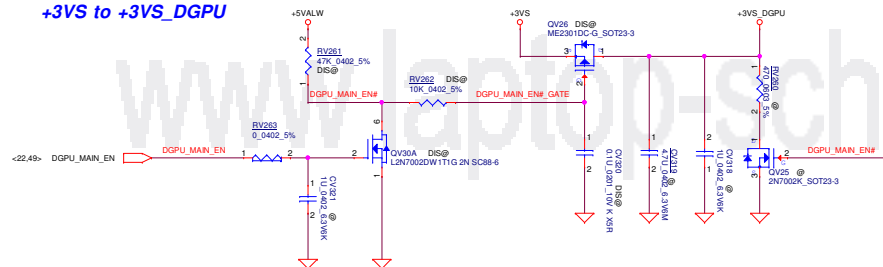


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Size		Document Number		Date		Wednesday, June 21, 2017		Sheet		20 of 51	
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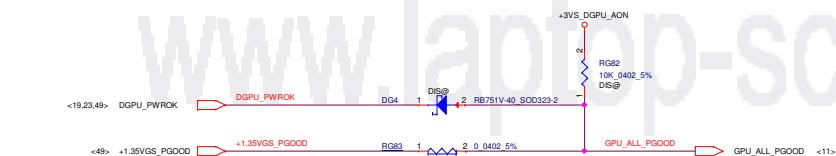
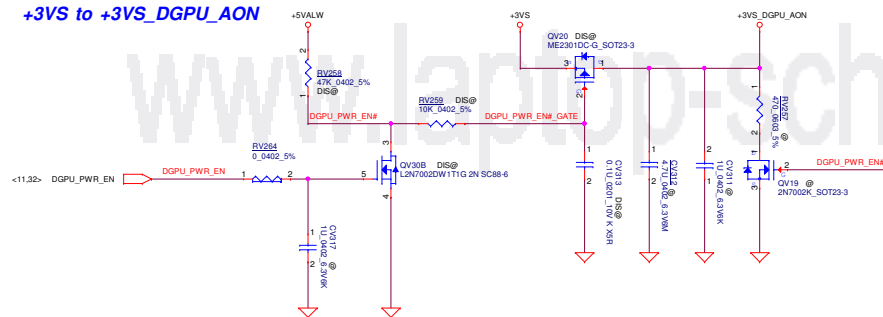


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					LA-E541P	2A
Date:				Wednesday, June 21, 2017	Sheet	21 of 51

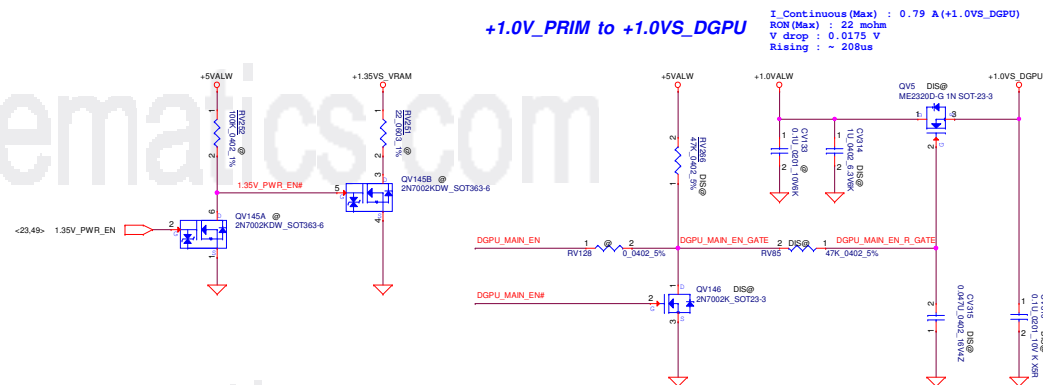
+3VS to +3VS_DGPU



+3VS to +3VS_DGPU_AON

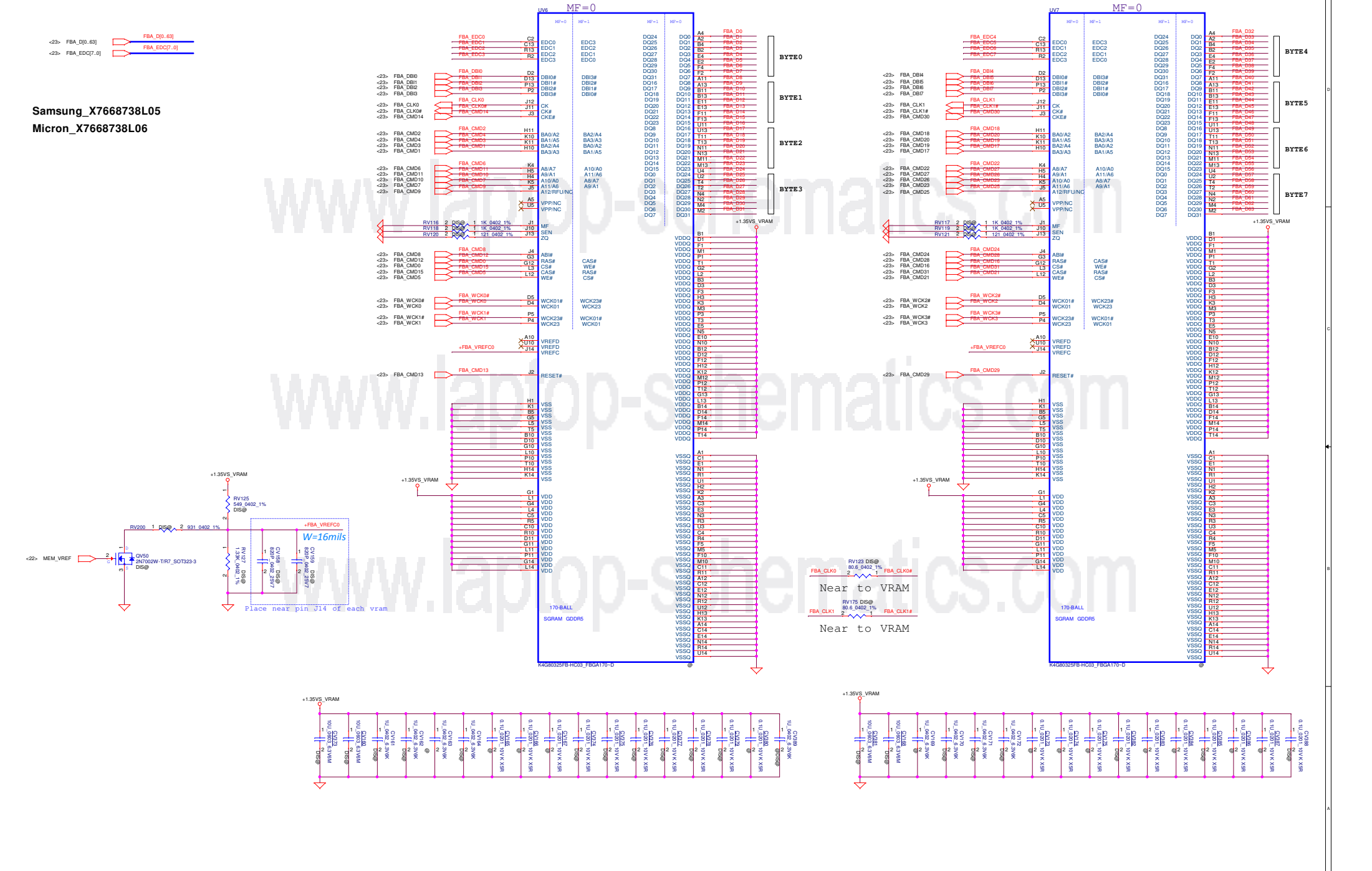


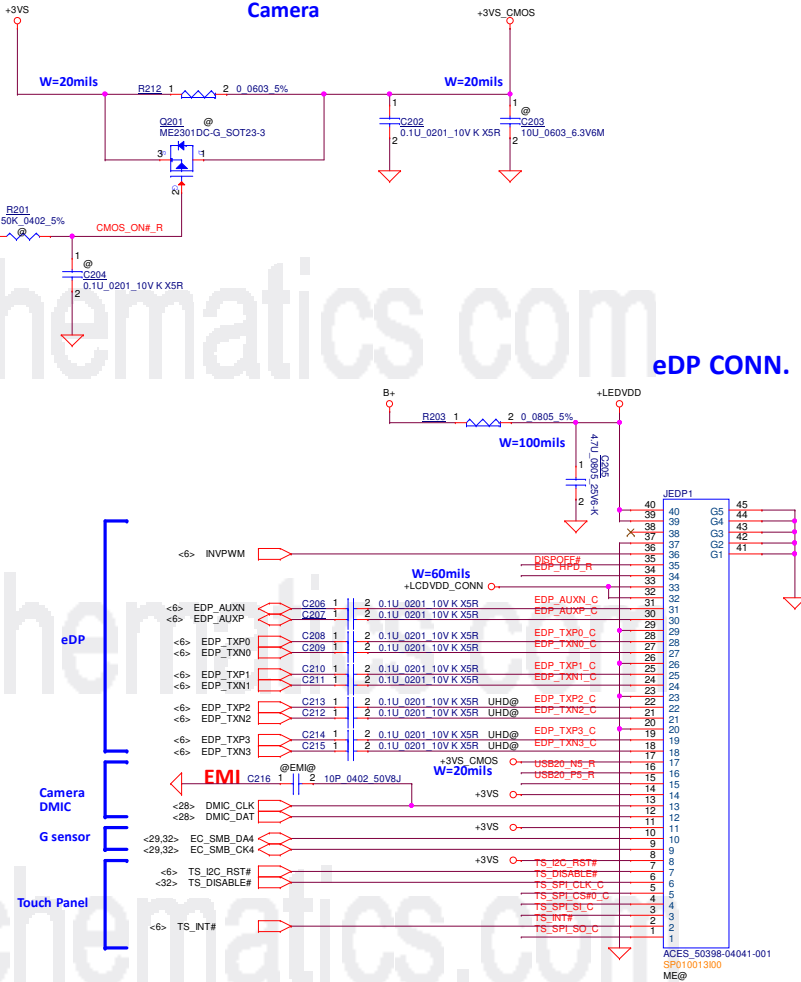
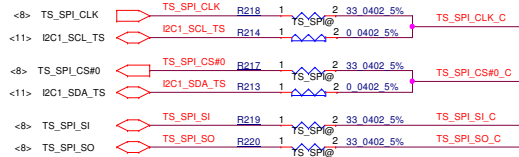
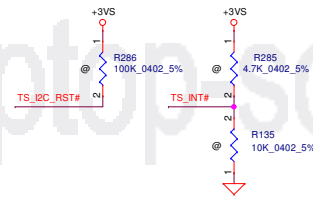
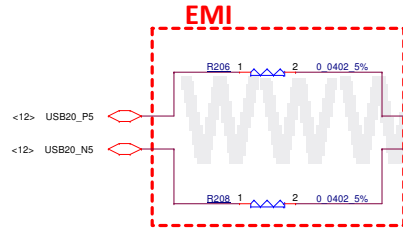
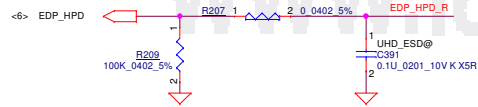
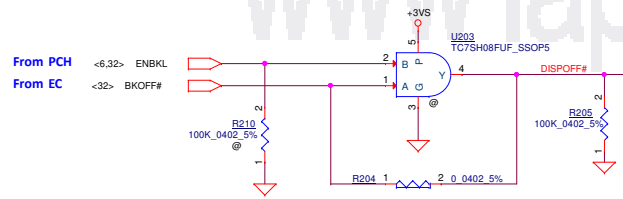
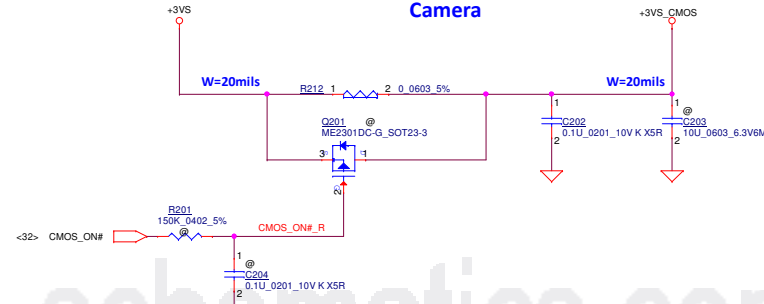
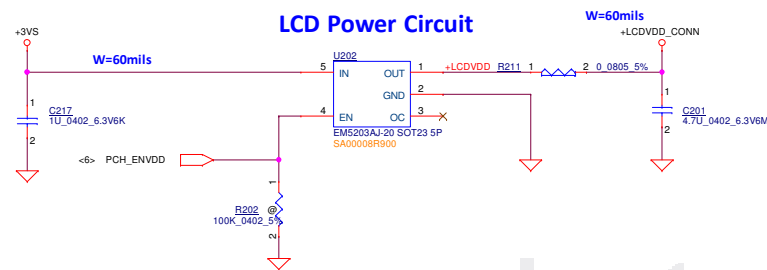
+1.0V_PRIM to +1.0VS_DGPU



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				DGPU DC/DC Interface	
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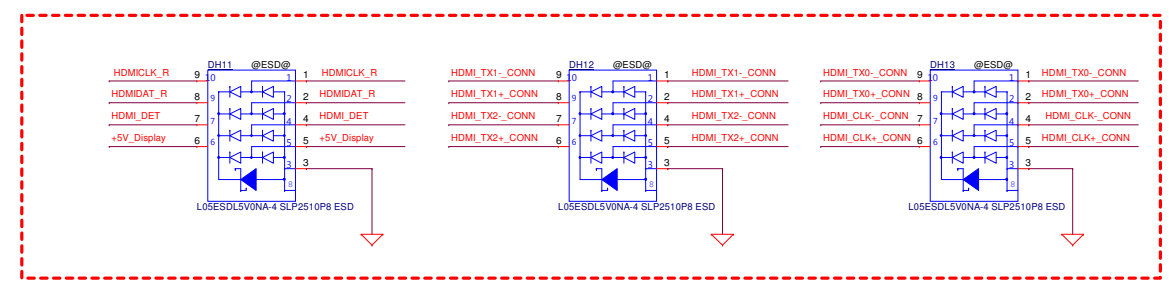
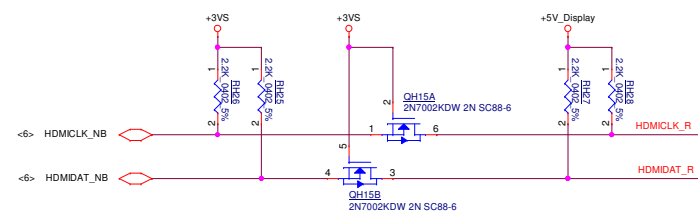
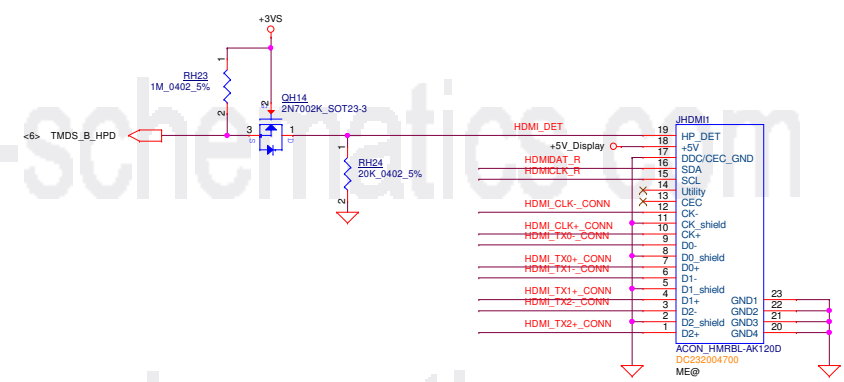
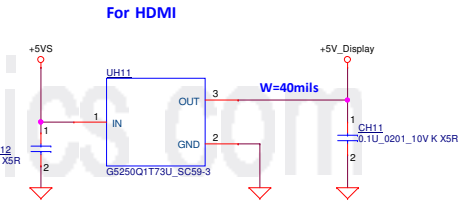
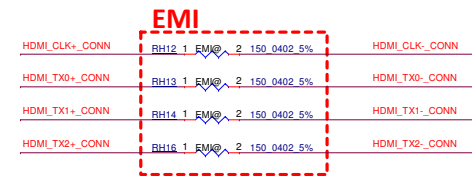
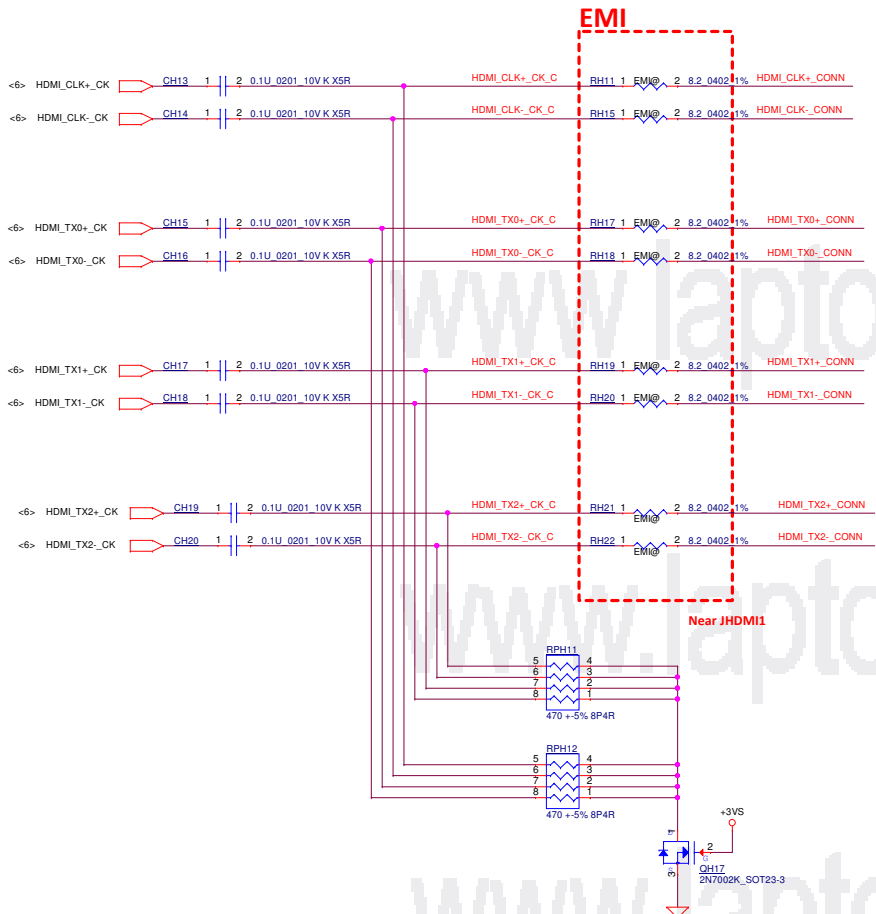
Memory Partition A





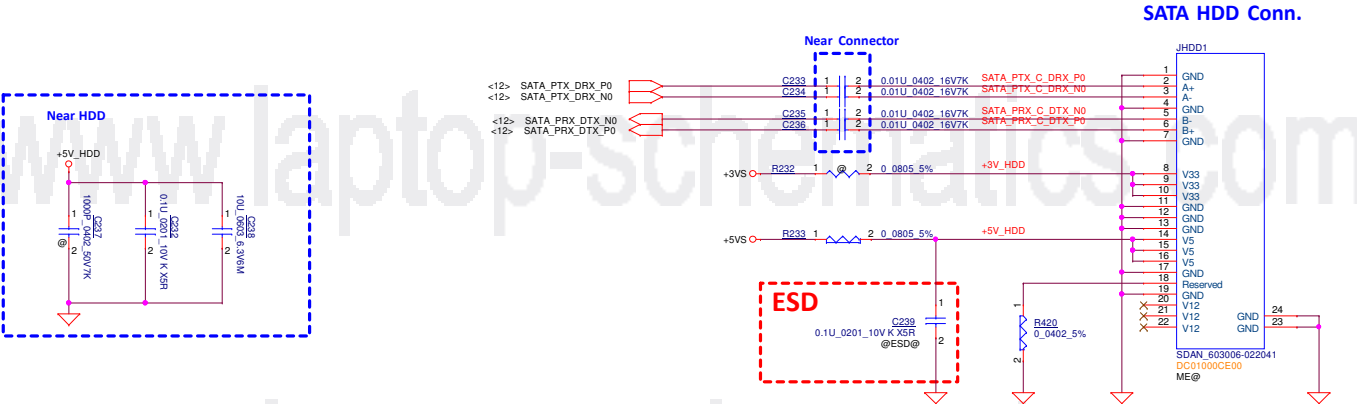
Elan Precise select by BOM (10 pins)		
1	PWR	PWR
2	CS	SCL
3	SCK	SDA
4	MOSI	Report switch
5	MISO	INT
6	Report switch	Reset
7	INT	Hsync
8	Reset	GND
9	Hsync	
10	GND	
Total	SPI (10 pins)	I2C (8 pins)

SPI & I2C PIN define		
1	PWR	
2	SPI_Reset/I2C_Reset	
3	Report_switch	
4	GND	
5	SPI_SCK/I2C_SCL	
6	SPI_CS/I2C_SDA	
7	SPI_MOSI	
8	SPI_INT/I2C_INT	
9	SPI_MISO	
10	GND	

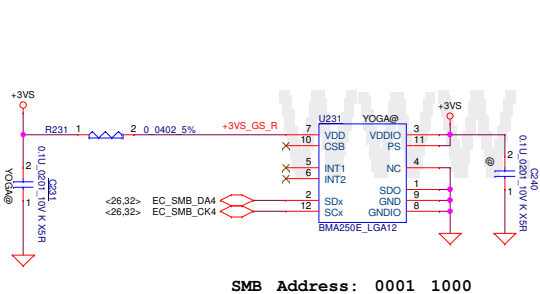


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				Size	Document Number
				Custom	LA-E541P
				Date: Wednesday, June 21, 2017	Rev 2A
				Sheet 27 of 51	

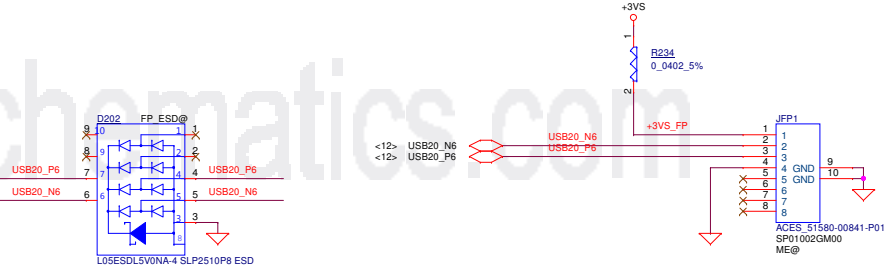
HDD



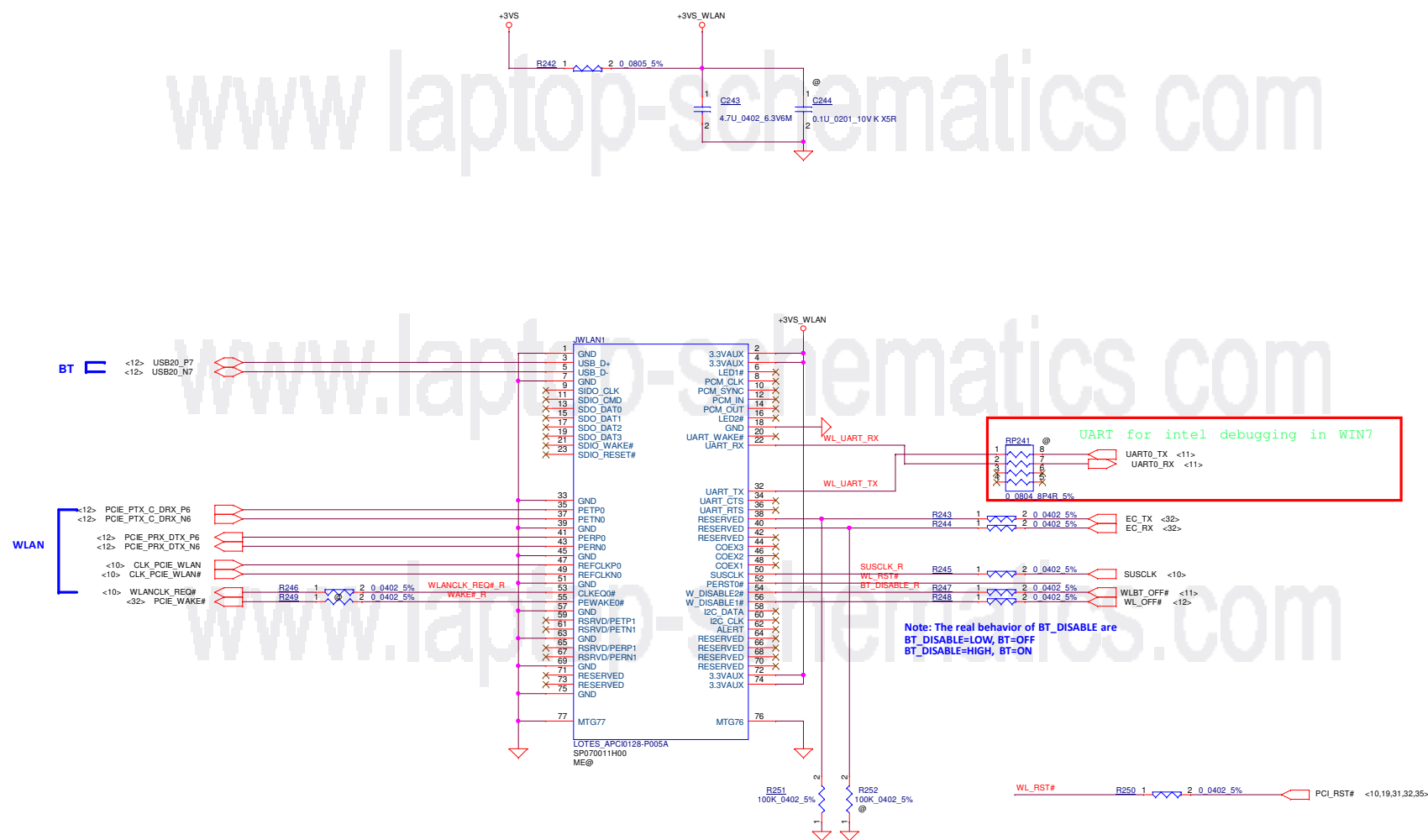
(G-Sensor for 360-degree reverse)



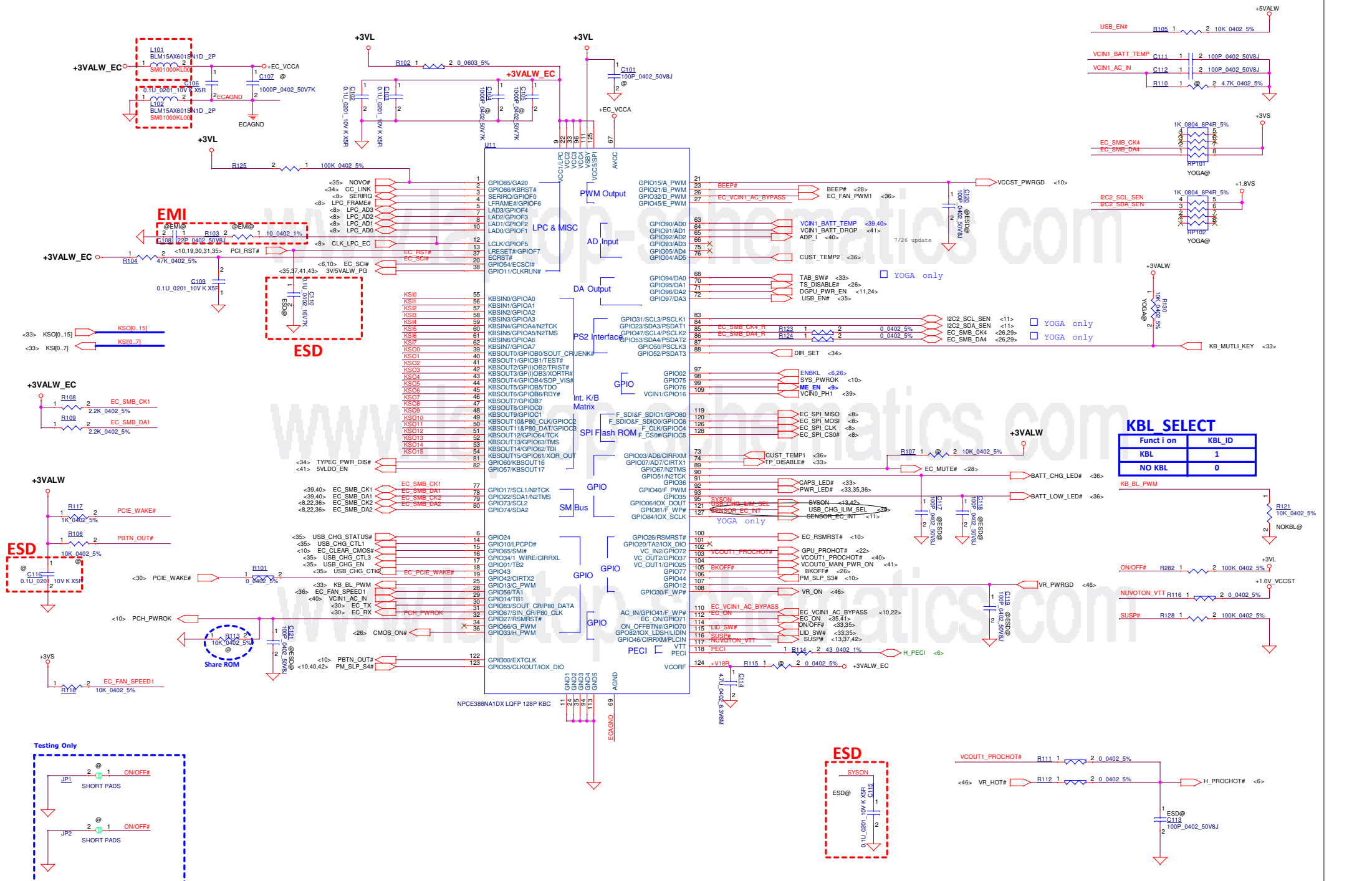
Finger Printer



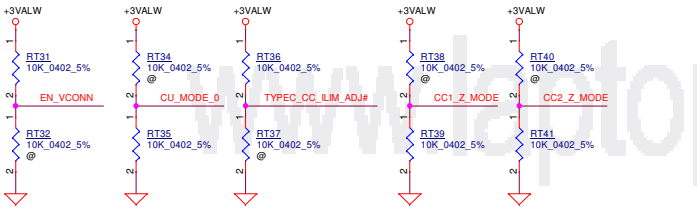
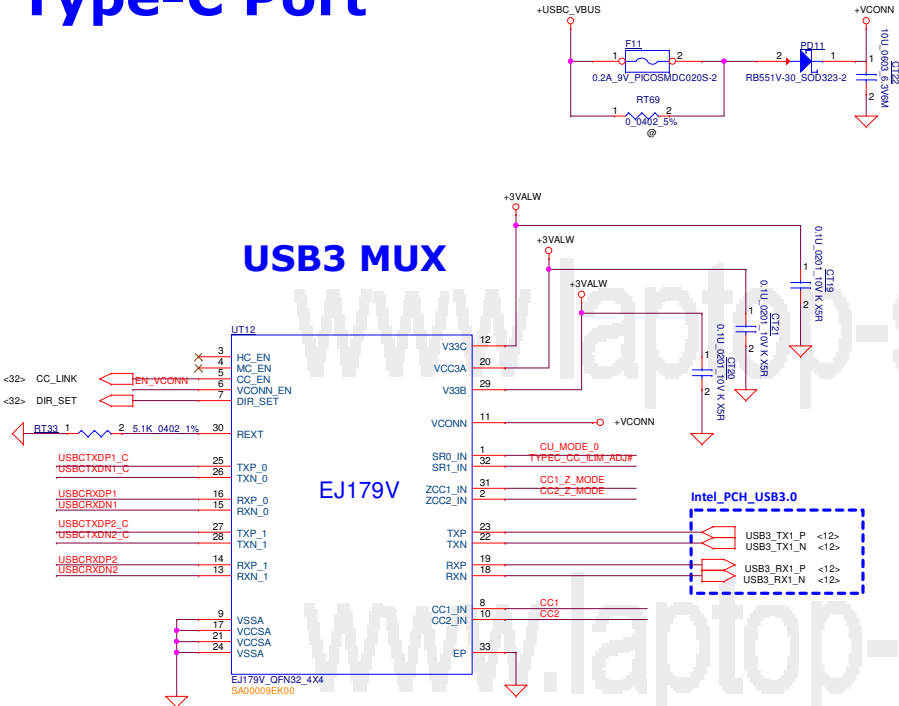
NGFF for WLAN / BT (E- KEY)



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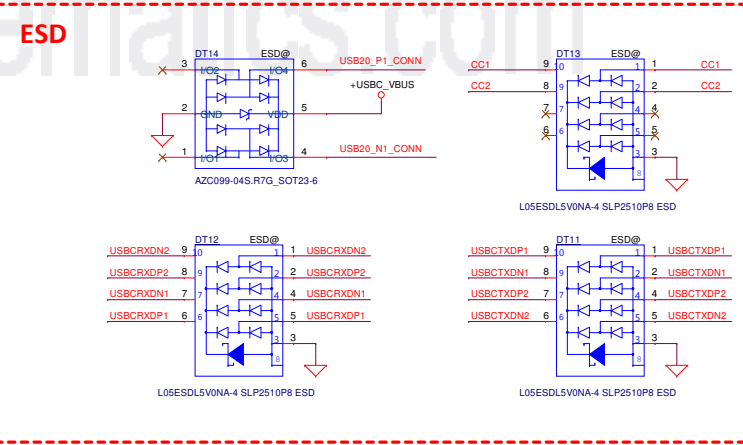
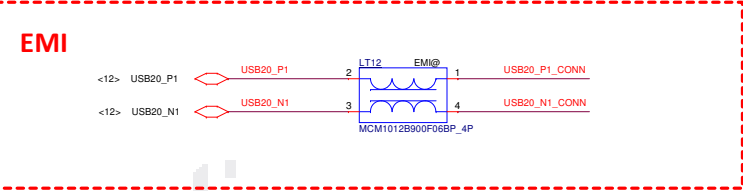
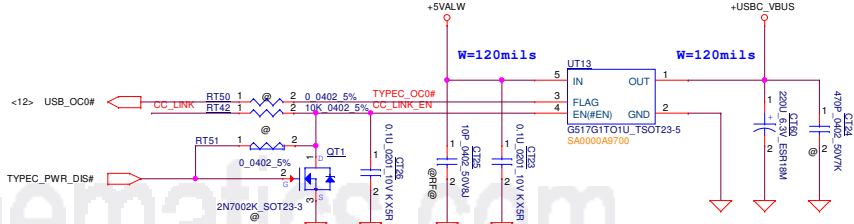
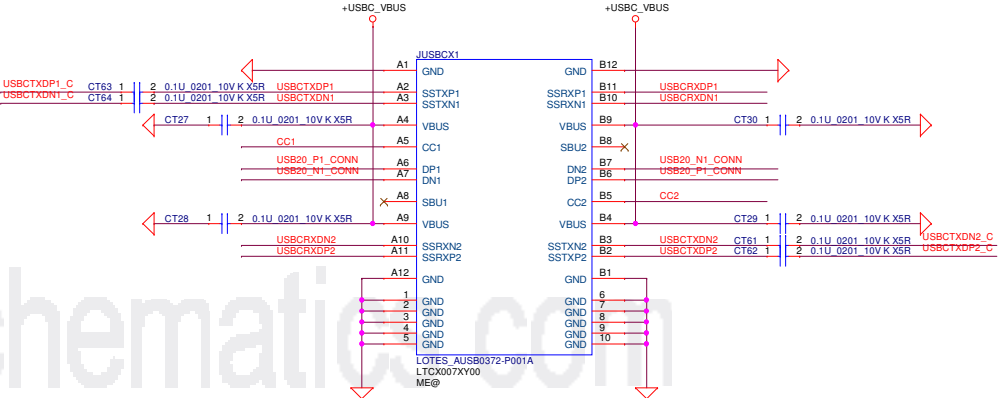
USB Type-C Port



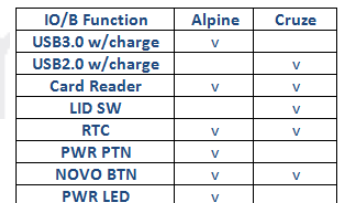
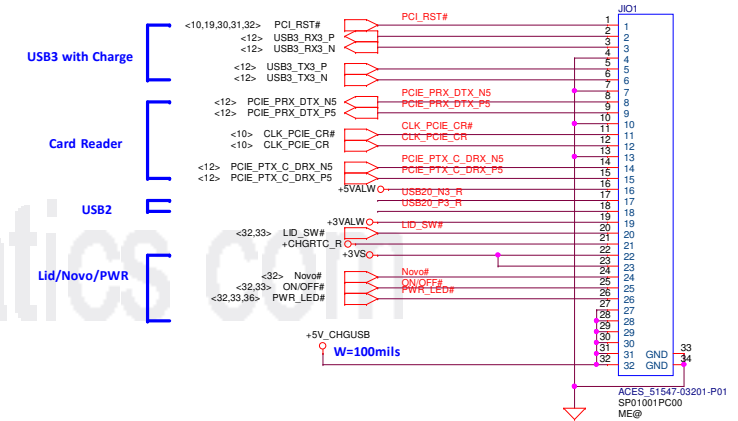
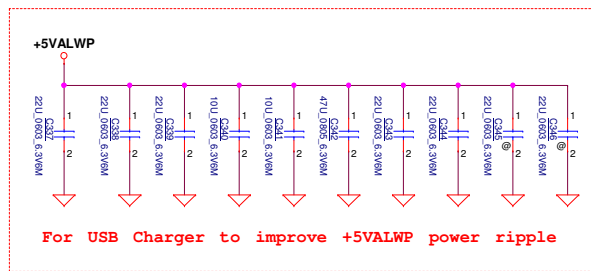
Profile Selection

EN_VCONN	CU_MODE_0	TYPEC_CC_ILIM_ADJ#	CC[1:2]_Z_MODE	CURRNET SELECT
1	0	0	00	DFP 900mA
1	1	0	00	DFP 1.5A
1	0	1	00	DFP 3A
0	1	1	00	UFP
0	X	X	01 10 11	EXTERNAL RESISTOR

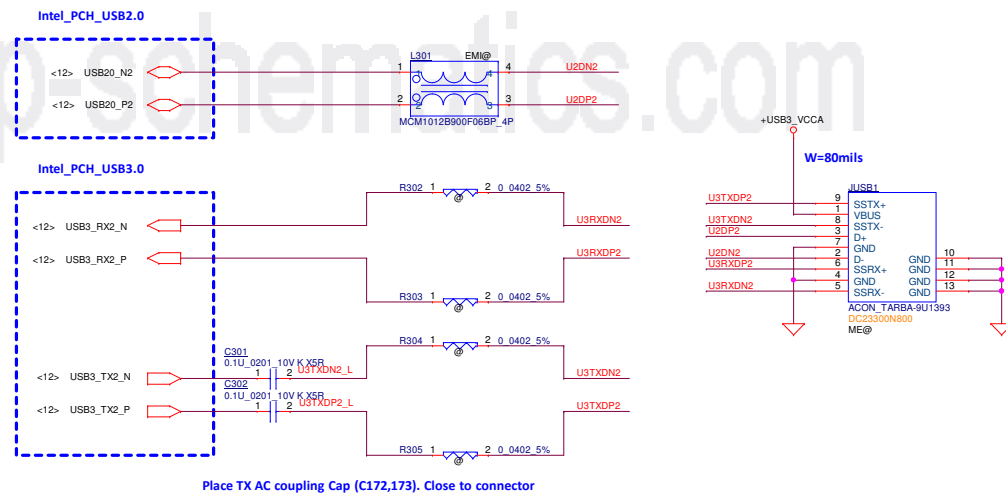
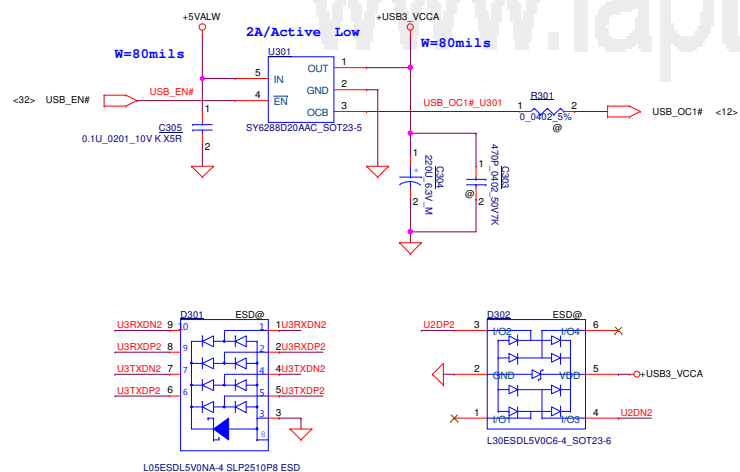
Currently setting



USB Charge

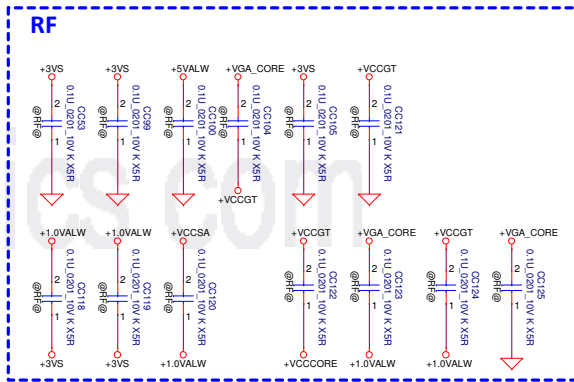
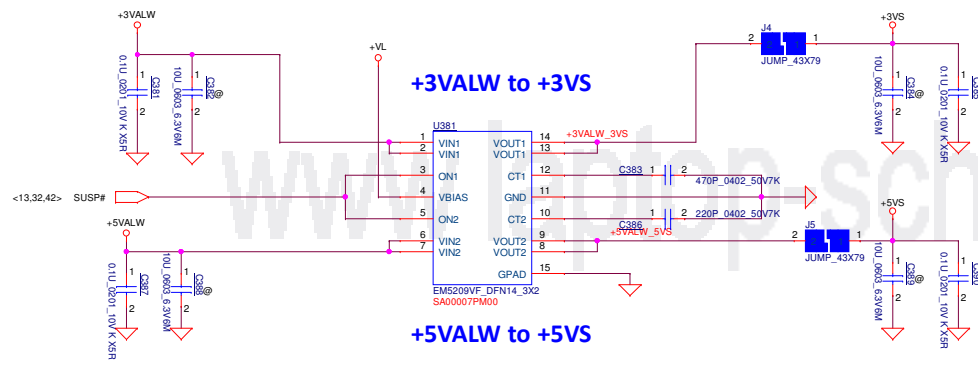


USB3.0_Port



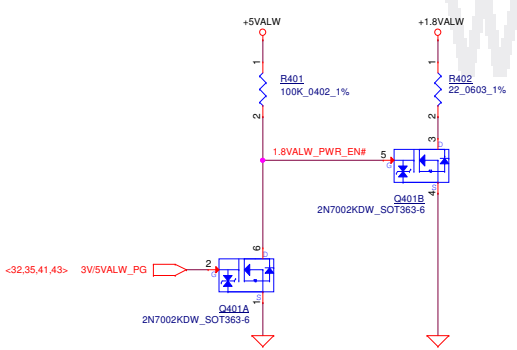
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				Size	Document Number
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DC to DC

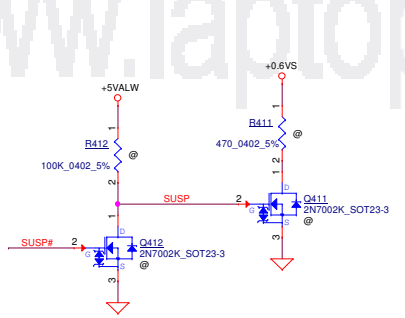


Discharge

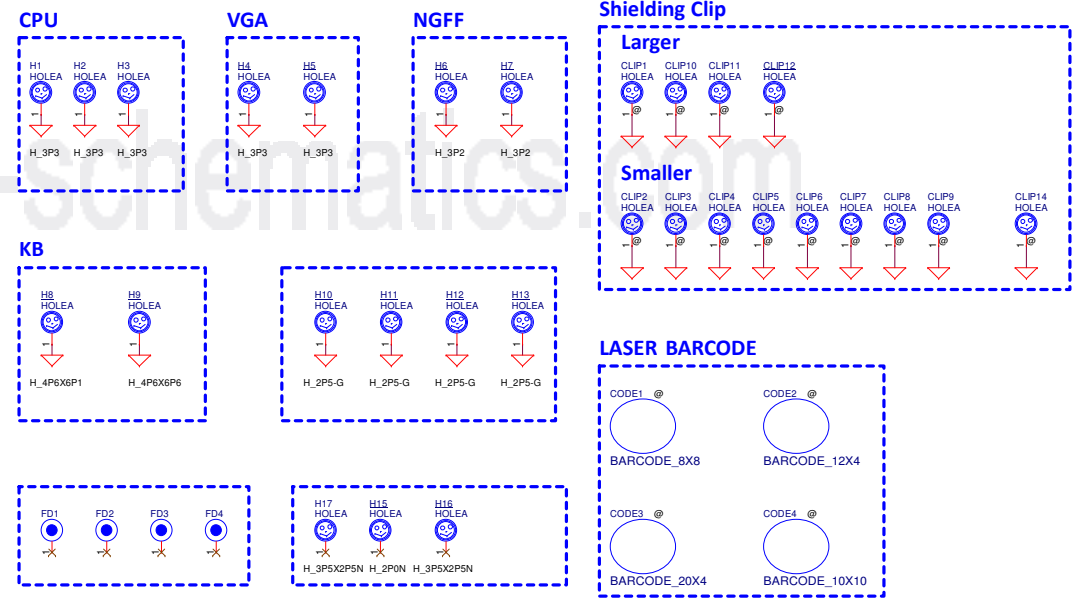
For +1.8VALW Discharge



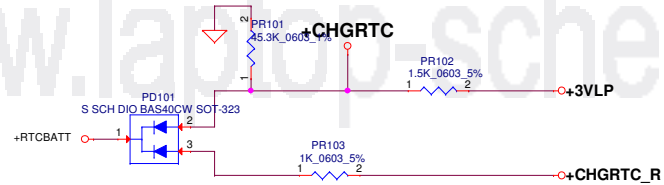
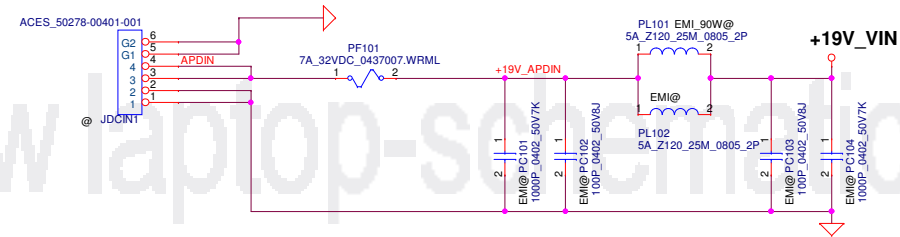
For +0.6VS Discharge



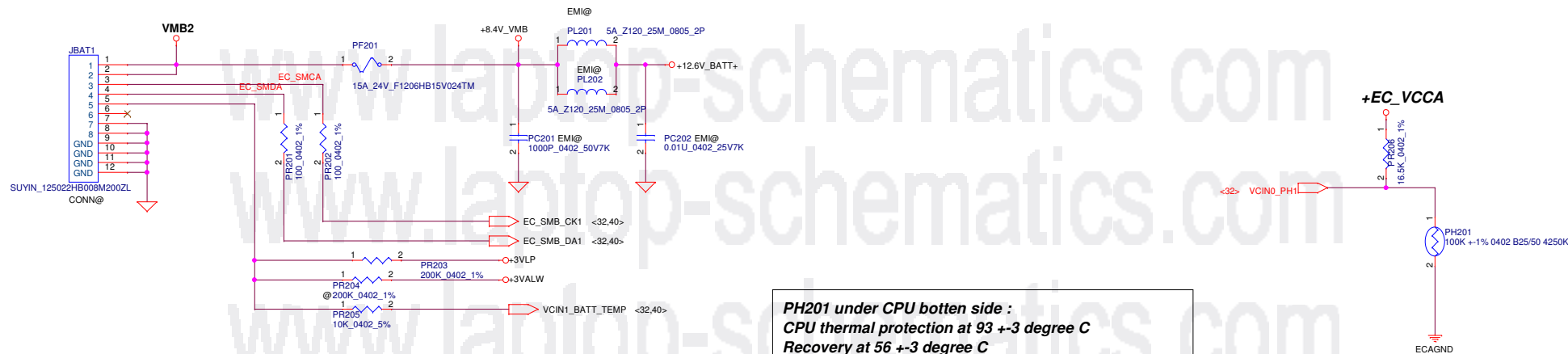
Screw Hold



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Size		Document Number		Rev	
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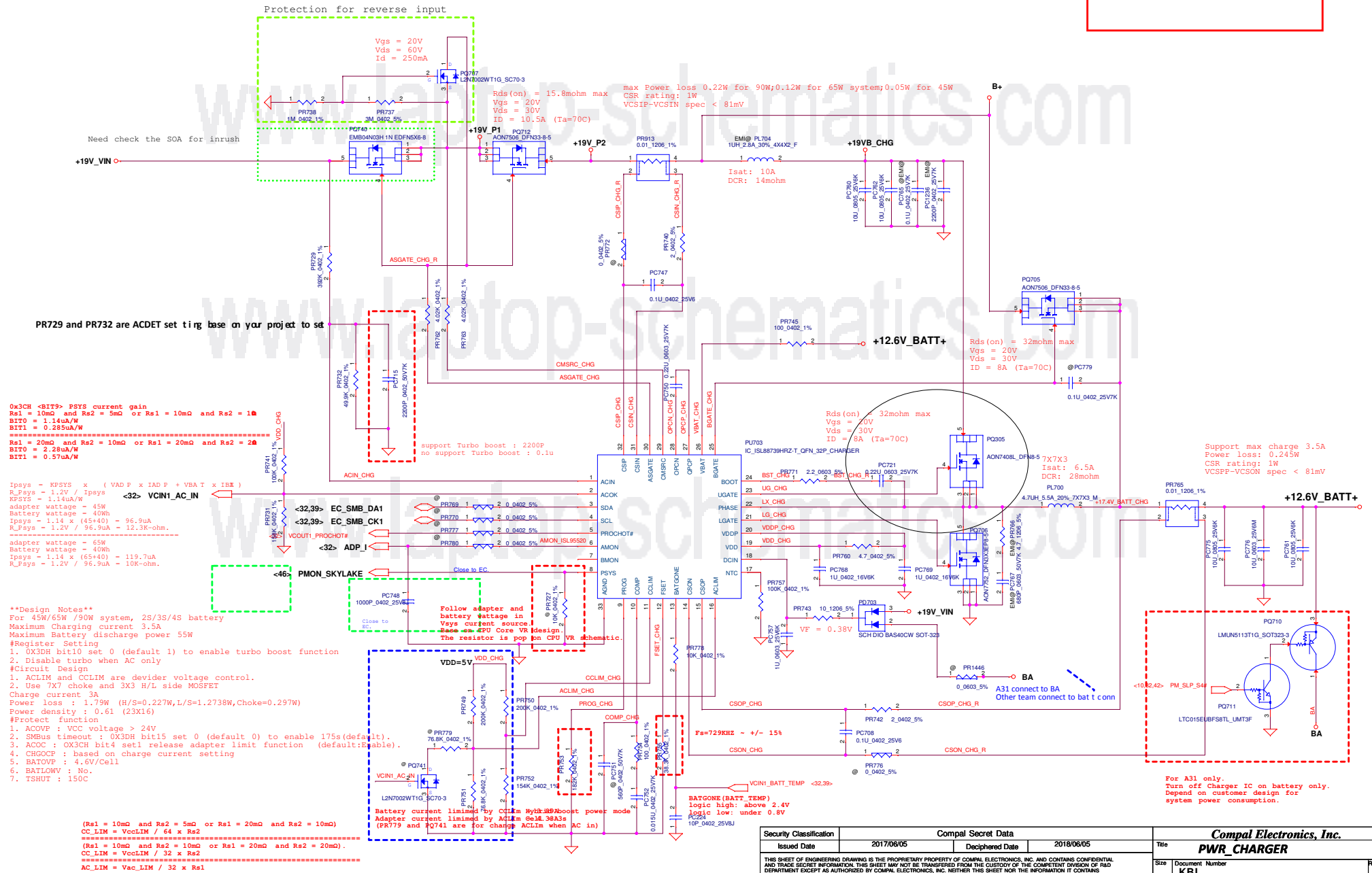


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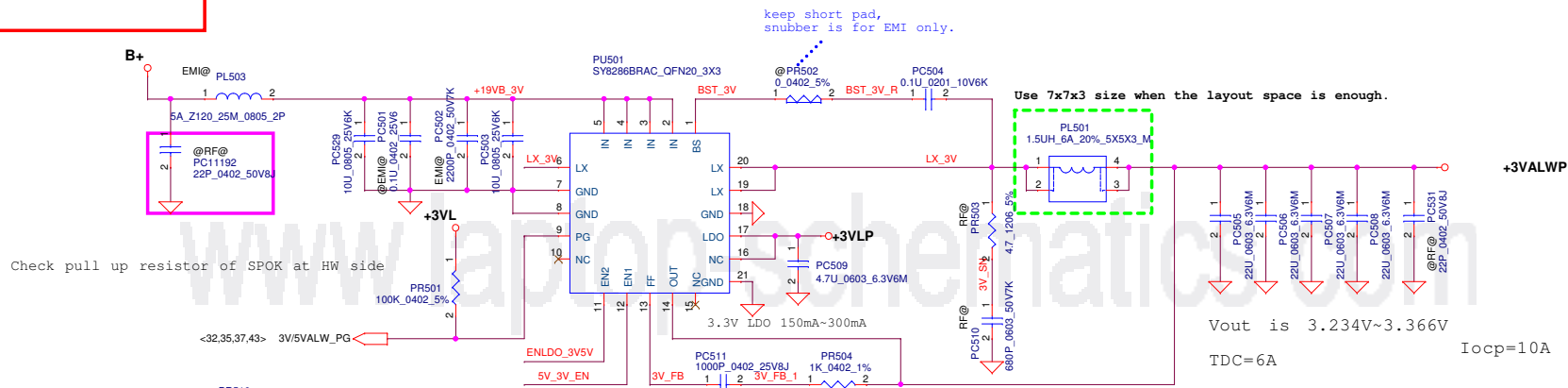
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Module model information
ISL95520_Hybrid_Boost_V2.mdd



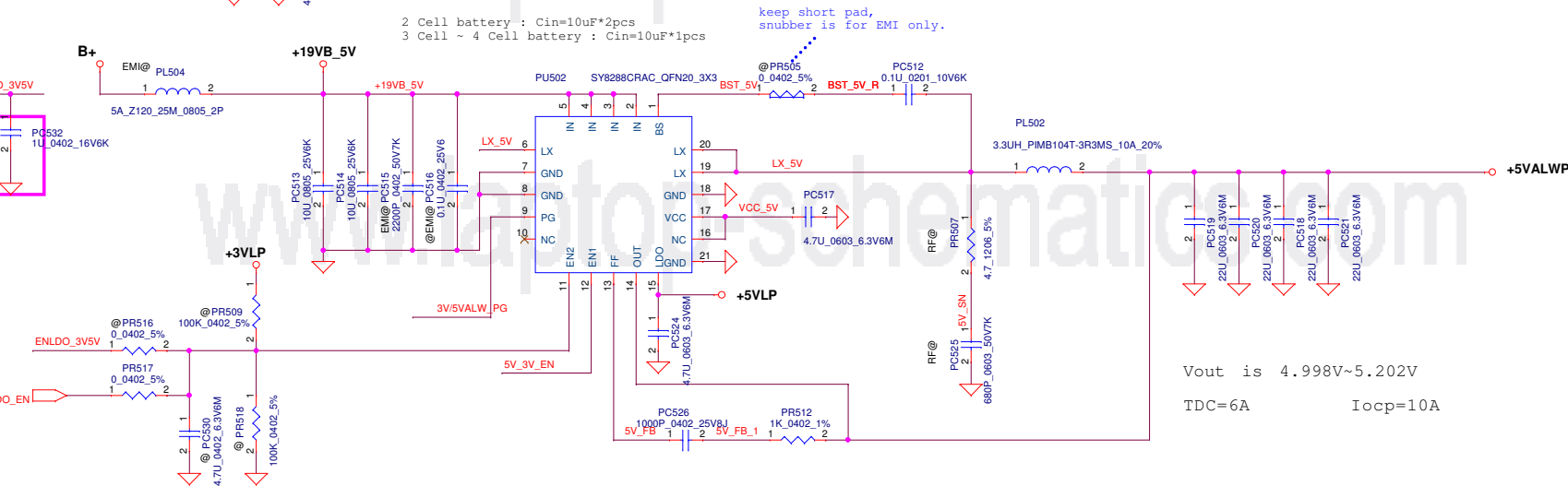
Module model information

SY8286B_V3_single.mdd
SY8286B_V3_dual.mdd



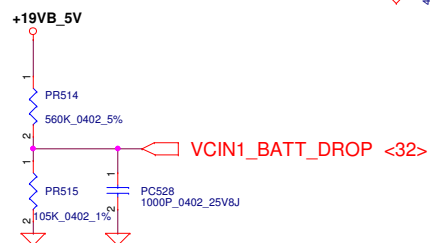
+3VALWP

+3VLP



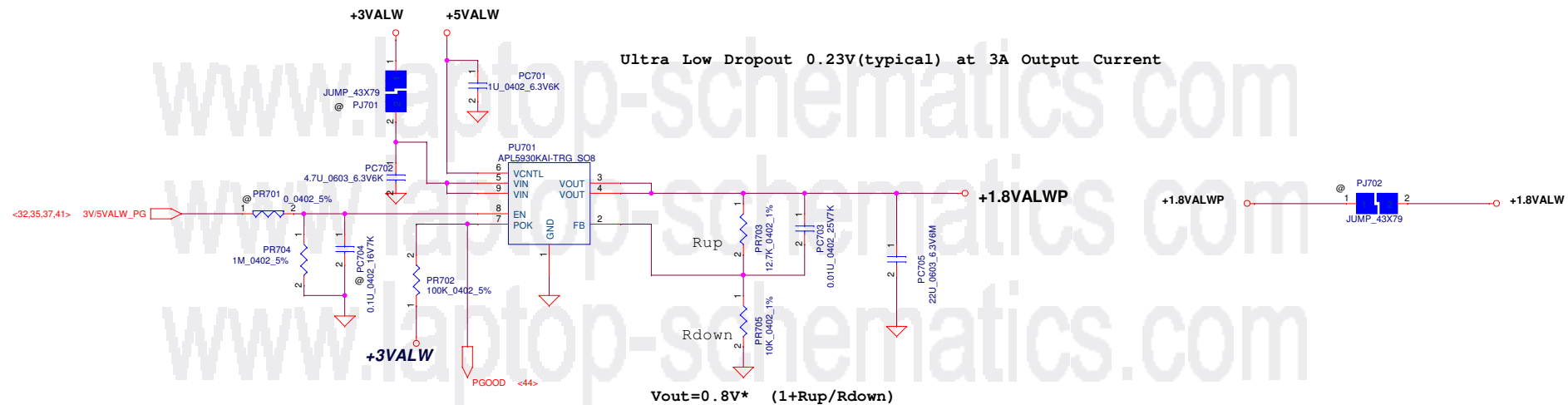
+5VALWP

+5VLP



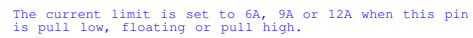
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APL5930_V2.mdd

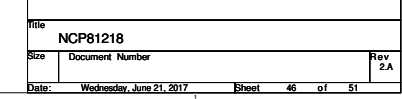


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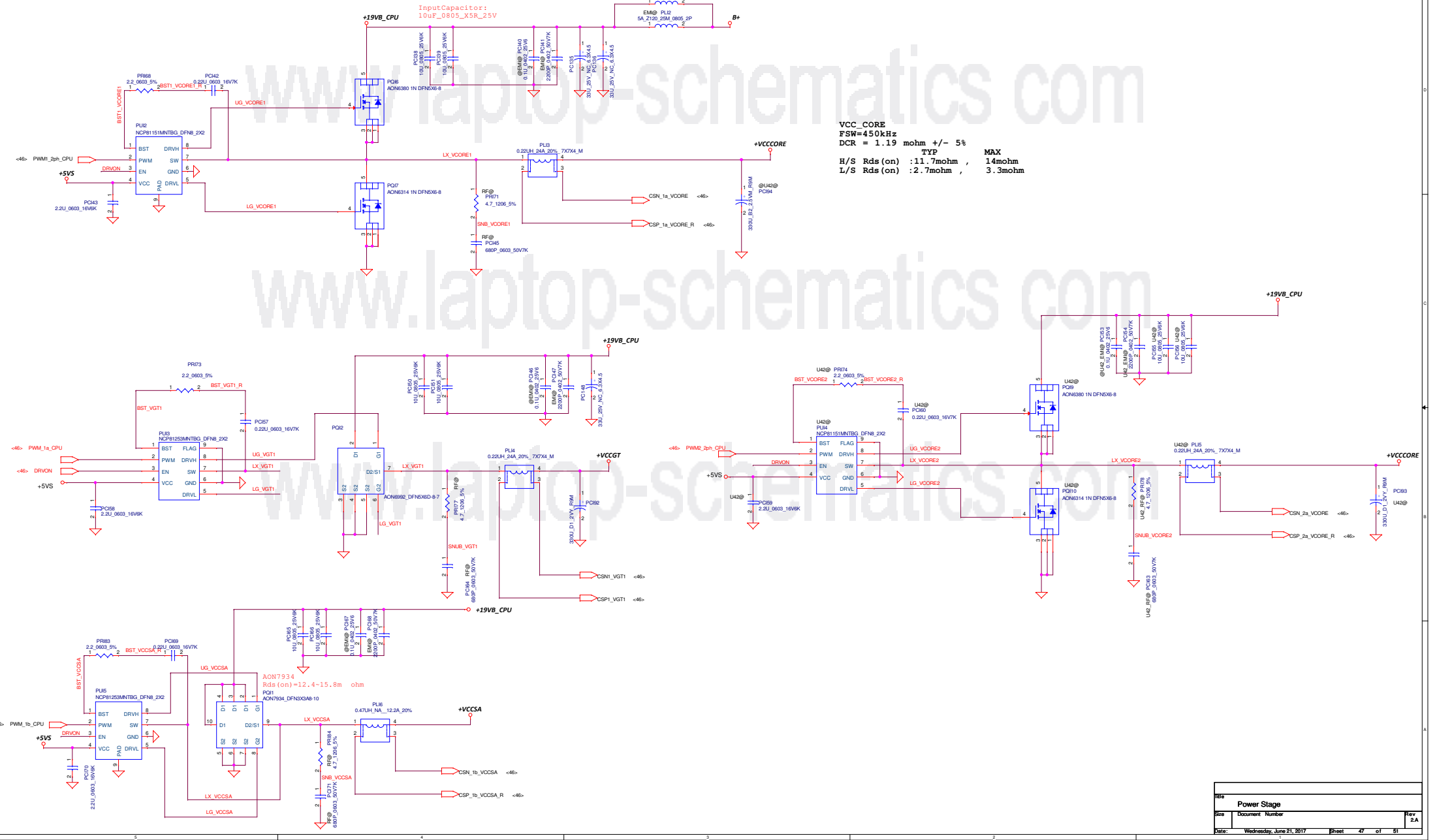
SY8286_V1_single.mdd
SY8286_V1_dual.mdd



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CPU POWER STAGES

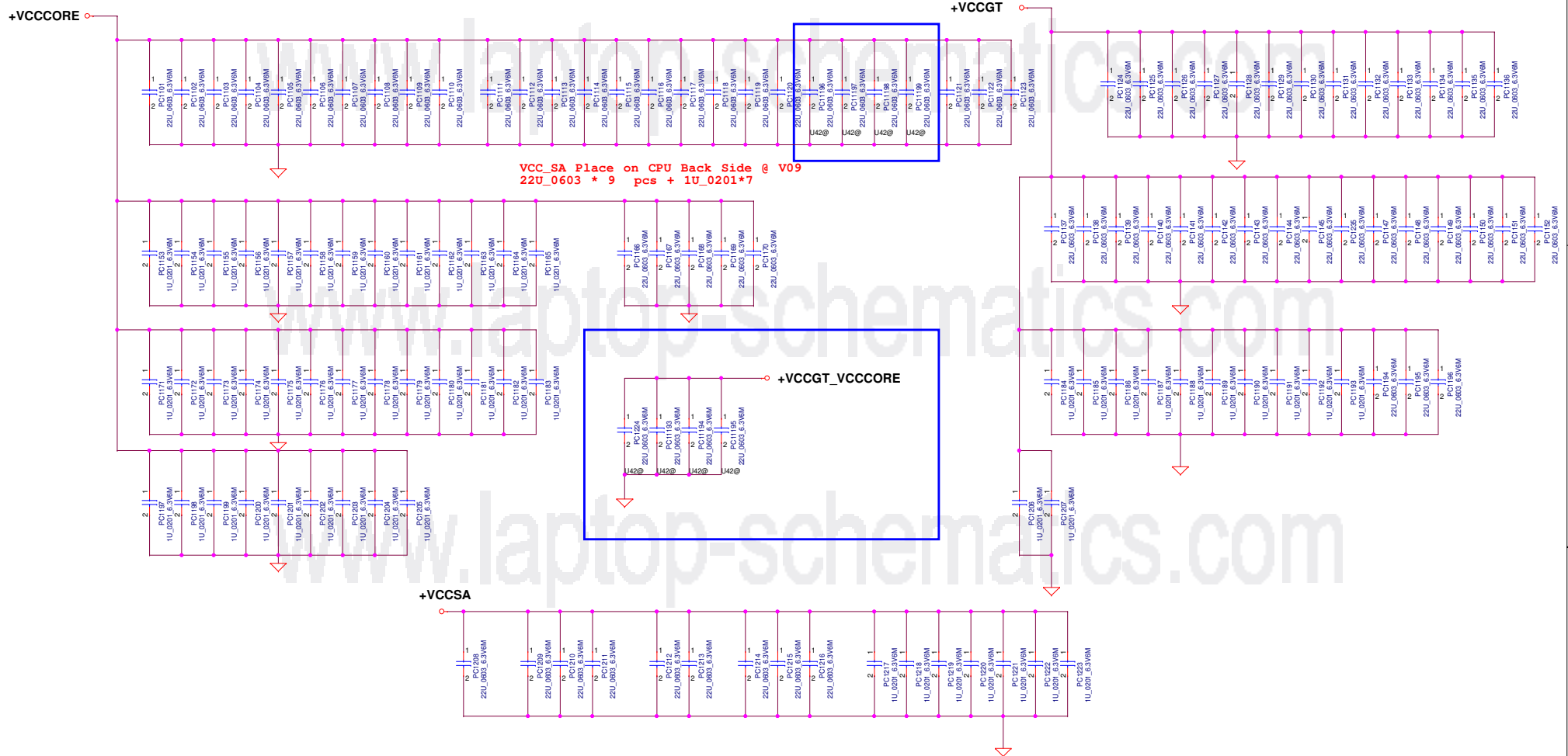


VCC_CORE
FSW=450kHz
DCR = 1.19 mohm +/- 5%
H/S Rds(on) :11.7mohm , MAX 14mohm
L/S Rds(on) :2.7mohm , 3.3mohm

Power Stage		
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VCC_CORE Place on CPU Back Side @ V09
22U_0603 * 36pcs +1U_0201*35 pcs

VCC_GT Place on CPU Back Side @ V09
22U_0603 * 32 pcs +1U_0201*12 pcs



PWM-VID Spec	Config A	Config B	Config C
Vmin	0.6V	0.6V	0.65V
Vmax	1.2V	1.2V	1.15V
Vboot	0.875V	0.9V	0.9V
Voltage step	6.25mV	6.25mV	25mV
N of voltage steps	96	96	20
Pr8	39K	20K	39K
Pr7	39K	20K	30K
Pr10	1.5K	2K	3K
Pr20	30K	18K	24K
Pr21	1.5K	0	3K
PrC9	1.5m	2.7n	1.8n

PWM VID and Output voltage control

- 1.Boot mode
- 2.Standby mode (don't support)
- 3.Normal mode

